Direct Memory Access Controller Design and Implementation for decreasing the Memory Access Time, Power and Area

Santosh Kumar B
CSE , New Horizon College of Engineering, Bengaluru, Karnataka, India

***Abstract*— Most of the newly developed stand alone embedded devices in the field of image, video and sound processing take more and more use of direct memory access controller. This controller is focused at high transmission capacity applications, for example, live video streaming. It is intended to drive 256-bit double data rate synchronous dynamic random access memory. The double data rate synchronous dynamic random access memory architecture utilizes a 2n-prefetch architecture, where the inner information transport is double the width of the outer information transport. A solitary read or compose cycle includes a solitary 2n-bit wide, one-clock-cycle information exchange at the center, and two relating n-bit wide, one-half-clock-cycle information exchanges at the I/O. Hence, this empowers fast activity as the inside section gets to are half the recurrence of the outer information exchange rate. Double data rate synchronous dynamic random access memories utilize a byte-wide, bidirectional information strobe that is transmitted remotely, alongside information (DQ) for information catch. Bidirectional information strobe is transmitted edge-adjusted by the double data rate synchronous dynamic random access memory amid peruses, and focus adjusted by the controller amid keeps in touch with the memory. The double data rate synchronous dynamic random access memory uses on-chip delay-bolted circles to check out bidirectional information strobe and comparing DQs, guaranteeing that they are very much coordinated and that they track each other with changes in voltage and temperature. For FPGA structure the IC producers are giving business memory controller IP centers working just on their items. Principle impediment is the absence of memory get to enhancement for arbitrary memory get to designs. The 'data path' some portion of those controllers can be utilized free of charge. This work propose a design of a double data rate synchronous dynamic random access memory controller, which exploits those accessible and well tested data paths and can be utilized for any reconfigurable device.**

***Keywords* - *Xilinx ISE, Direct Memory Access Controller,* bidirectional information strobe.**

I. INTRODUCTION

The extending execution hole among processors and memory has made the memory subsystem one of the restricting variables of a broadly useful PC framework's execution. This marvel has been named the Memory Wall. Present day memory frameworks for the most part have huge data transfer capacities and this is regularly thought of as having the capacity to adjust for substantial memory latencies. This might be valid for applications where vast information streams are utilized, (for example, media processing), yet the accessibility of transfer speed alone can't lessen all memory latencies. Since memory advancements are probably not going to change definitely as far as their speed, more spotlight is normally put on changing the association and interface of the memory to grow new memory plans. We are extraordinarily choosing memory type SDRAM as synchronous dynamic random access memory and DDR recollections are for the most part utilized in memory structures of installed frameworks as it is helped with fast, burst access, pipelining, versatility and legitimate order instatement.

II. PROPOSED DIRECT MEMORY ACCESS CONTOLLER

This controller is focused at high data transmission applications, for example, live video handling. It is intended to drive 32-bit double data rate synchronous dynamic random access memory. The memory substance are gotten to through a 64-bit FML (Fast Memory Link) transport with a burst length of 4. FML is a blasted arranged transport intended to facilitate the plan of DRAM controllers. Its signaling resembles WISHBONE, but basically removes all corner cases with burst modes to save on logic resources.

III. ARCHITECTURE OF DIRECT MEMORY ACCESS CONTROLLER

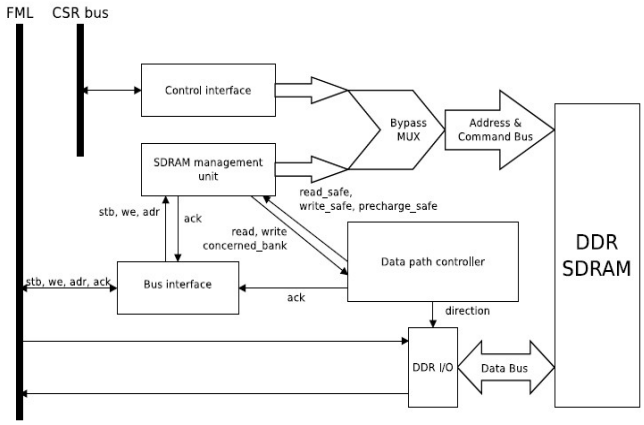

Fig. 3.1: Block-diagram of proposed high performance SDRAM Controller

High performance direct memory access controller gives high flexibility and reserve funds on equipment by actualizing a detour mode which gives the CPU low-level access to the synchronous dynamic random access memory direction interface (address pins, bank address pins, and CKE, CS, WE, CAS and RAS). The synchronous dynamic random access memory instatement grouping is appointed to the CPU, which should utilize this mode to actualize it. Timing parameters are likewise configurable at runtime. These control interfaces are gotten to on a 32-bit CSR transport, separate from the information transport.

3.1 Fast Memory Link

The Fast Memory Link transport is intended to give a superior interface between a DRA controller and peripherals that need to get to a lot of data.FML transports are alluded to asbxw FML; which implies that the transport works with a burst length of b and that the width (in bits) of each unidirectional information line is w.

Fast Memory Link (FML) transport highlights:

- Synchronism. The transport is intended to be utilized in FPGA-based gadgets, whose structures are intended for synchronous frameworks.
- Burst situated. Each cycle starts with a location stage, which is then trailed by a few information pieces which are exchanged on continuous clock edges (the information stage). The length of the burst is fixed.
- Pipelined exchanges. Amid the information period of a cycle, the control lines are free and can be utilized to start the location period of the following cycle.

IV. RESULTS OF DYNAMIC ACCESS MEMORY CONTROLLER

At the point when the framework is controlled up, HPDMC comes up in bypass mode and the SDRAM instatement arrangement ought to be performed from that point, by controlling the pins at a low level utilizing the bypass register. The SDRAM must be modified to utilize a fixed burst length of 8, and a CAS inertness of 2 or 3, CAS latency 2.5 is not upheld.

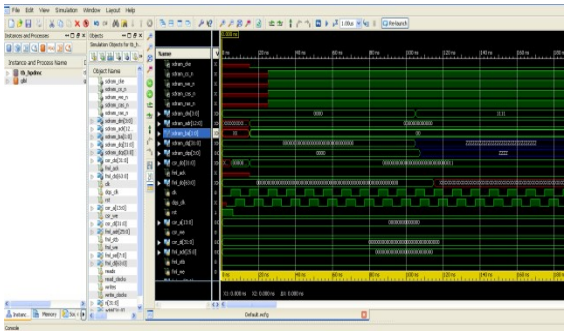

Fig 4.1: Simulation output of high performance direct access memory controller

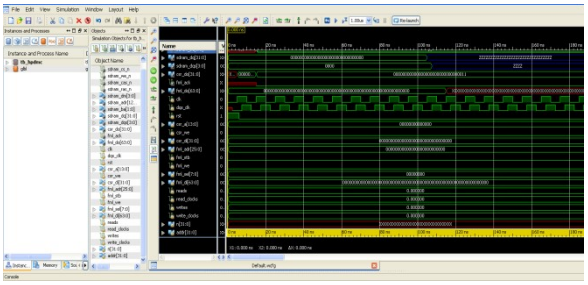

Fig 4.2: Simulation output of high performance direct access memory controller

V. CONCLUSION AND FUTURE WORK

The after effects of the experimentation utilizing a sensible portrayal of an equipment configuration have uncovered a few bits of knowledge into the execution of a double data rate synchronous dynamic random access memory framework and the controller utilized in such a framework.

Table I: Comparison table for existing and proposed model

Parameters	Existing Model	Proposed Model
Power Supply	1.8 + 0.1 V	1.7 + 0.1 V
Area	29mm	27mm
Delay	2.5ns	2.4ns
Gate Count	64 million transistor	68 million transistor

Initially, some broad perceptions about double data rate synchronous dynamic random access memory based memory can be made. These perceptions, combined with the novel commitments of this work, can show where future work in the field ought to be done to additionally improve the execution of the memory framework, diminishing the memory get to time, power and region. The steady need to support memory execution for progressively ground-breaking framework processors drives the improvement of advanced memory technologies.

REFERENCES

[1] How to Use DDR SDRAM, User's Manual, Document No. E0234E40, ALPIDA, September 2005
[2] DDR SDRAM Controller Using Virtex-4 FPGA Devices, Oliver Despaux, Application Note, March 27, 2006.
[3] http://www.xilinx.com
[4] Double Data Rate (DDR) SDRAM Specification, JEDEC STANDARD, JESD79E, May 2005