Low Power Voltage Controlled Oscillator for PLL using Operational Transconductance Amplifier

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***Abstract:-*Voltage Controlled Oscillator (VCO) using Operational Transconductance Amplifier (OTA) for Phase Locked Loop (PLL) is designed in 180 nm technology. The designed VTO has a voltage to current converter (V-I converter), a Current Controlled Oscillator (CCO) and three CMOS inverters. The CCO design is based on single ended rail to rail OTA The free running frequency range of OTA based VCO is 60 to 435 MHz. The design of the circuit is done using Cadence VLSI design suite and this VCO is power efficient and would result in a low cost compact IC when fabricated.**

Keywords— Cadence VLSI design suite; OTA; PLL; VCO.

I. INTRODUCTION

Phase Locked Loop is one of the mostly used circuit for various applications such as clock generator for processors, in frequency synthesizer, in FM demodulating circuit ect. [1].

It is used to generate high frequency stable output signal from a fixed low-frequency signal.

A PLL is a combination of Phase Frequency Detector (PFD), Charge Pump, Loop Filter,

VCO, and a Frequency Divider (which is usually connected externally). Because of the frequency matching performance has to be performed by the VCO and it is the major part in PLL circuit, VCO decides the power consumed and area occupied by the PLL [1].

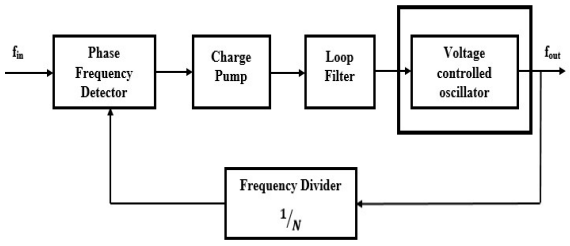

Fig 1: Block diagram of PLL

A VCO works with the principle of linearity between the output frequency and its control voltage. The conventional way of designing a VCO using odd number of inverters; hence the supply voltages of the inverters determine the output frequency of the VCO. It causes difficulty in controlling the output frequency. To overcome this major disadvantage, in this paper, the concept of OTA based VCO is introduced. where OTA act as a buffer, helps in giving a full control on the output frequency [2].

The major unites of VCO designed here are voltage to current converter (V-I converter) and a Current Controlled Oscillator (CCO). Cadence 180nm technology with supply voltage 1.8V has been used for the simulation of the circuits at schematic and layout level. The working of PLL is analysed under different test conditions.

The designed VCO has an operating frequency range from 60 to 435MHz. This frequency range is compactable for the PLLs to use as the clock generator for microprocessors. Compared to the conventional ring oscillator, the PLL designed here is found to have better frequency control. Also VCO designed in this work has compact size and consumes less power, which resulted in the optimization of size and also reduces the power consumption of the PLL.

II. SEGMENTS OF PLL

PLL is a combinational circuit of four segments. It consists of Phase Frequency Detector, Charge Pump, Loop Filter and VCO. The block diagram of PLL is shown in Fig 1. PFD is a digital circuit that compares the frequencies of two signals- reference input frequency and feedback frequency - and produces the phase error as output. Charge pump is a capacitor-resistor combination circuit that charges or discharges the signal based on the lead or lag of the error signal. Loop filter is basically a low pass filter that removes high frequencies to stabilizing and smoothing the control voltage fed to it. The filtered error signal voltage form the Charge Pump; V_{cntrl}; is used as the control voltage for VCO. With respect to this error signal control voltage VCO output frequency varies positively of negatively. The frequency divider is an external control circuit which is used for controlling the VCO output frequency by varying the feedback signal frequency. The frequency divider divides the VCO output frequency by a factor of N to act as feedback signal.

III. VOLTAGE CONTROLLED OSCILLATOR

A Voltage to Current Converter (V-I converter) and a Current Controlled Oscillator (CCO) are two main circuits of a VCO, as shown in Fig 2. V-I converter converts its input voltage V_{cntrl} to a propositional current I_{bias}. The CCO functions to generate an output signal with a frequency corresponds to its

input current I_{bias}. In total, VCO generates a signal its frequency is proportional to V_{cntrl}[2]. Fig 3 shows the internal structure of a VCO. Here CCO has been implemented as a ring oscillator, which consists of feedback inverters, and OTA configured as buffer [2].

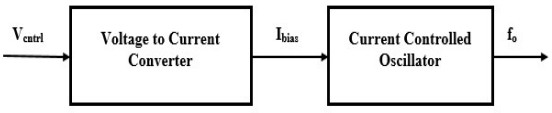

Fig 2: VCO block

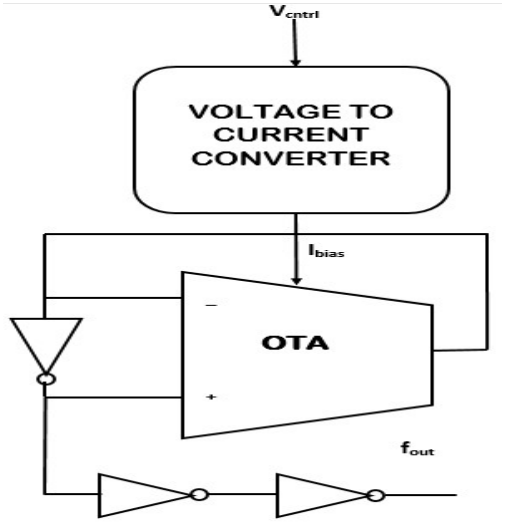

Fig 3: Internal structure of VCO

1. *Operational Transconductance Amplifier (OTA)*

An OTA is a Transconductance amplifer whose output "current" is proportional to the differences of two input "voltages". The functioning og this Voltage Controlled Current Source (VCCS) can be mathematically expressed as,

$$I_{out} = g_m(V_p - V_n) \qquad (2)$$

Where, g_m is the transconductance, V_p and V_n are the input voltages.

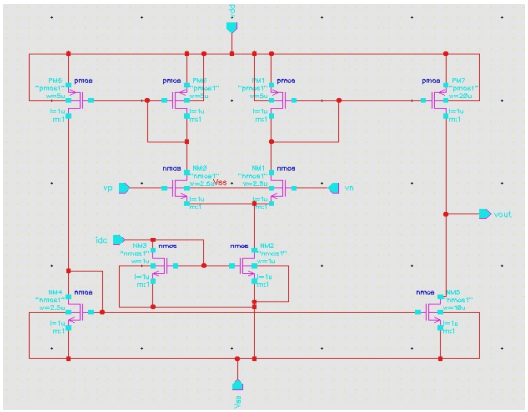

Fig 4: OTA schematic

From Fig 4, The term "1: K" indicates that the width of M4 and M5 can be sized K times wider (K>1) than the width of M41 and M51 respectively [5] [6]. All nodes are connected to gate, drain or source, except the input and output nodes.

The voltage gain is given by,

$$A_v = \frac{V_{out}}{V_p - V_n} \qquad (3)$$

The 3dB frequency is given by,

$$f_{3dB} = \frac{1}{2\pi r_{out} C_L} \qquad (4)$$

where, V_{out} is the output voltage

r_{out} is the output resistance

C_L is the load capacitance

From the OTA design the approximate frequency of oscillation of the CCO is given by

$$f_{out} = \delta\sqrt{I_{bias}} \qquad (5)$$

Equation (5) mathematically shows that the oscillation frequency of the designed CCO can be controlled from the OTA DC bias current.

2. *COMOS Inverter*

A PMOS and an NMOS in series with its drain terminals are shorted forms a CMOS inverter circuit. For the working, the source of PMOS and drain of NMOS should be connected to to V_{DD} and V_{SS} respectively. V_{in} is fed at the shorted gate terminals and the output V_{out} is taken from the shorted drain terminal as shown in Fig 5.

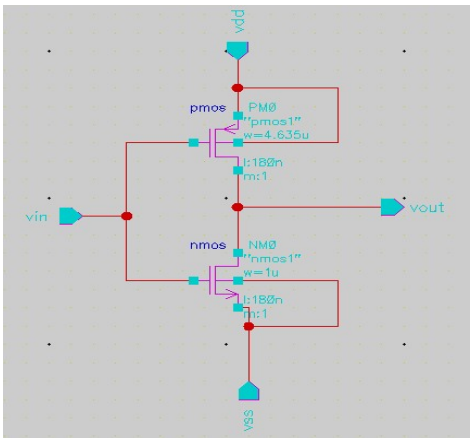

Fig 5: CMOS Inverter

3. *Current Controlled Oscillator (CCO)*

In CCO, the output signal frequency can be controlled using input current. The Current-Controlled Ring Oscillator mentioned here is based on a single-end rail-to-rail OTA and three CMOS inverters.

The oscillation frequency of the traditional ring oscillator cannot be easily controlled. But for a VCO, the frequency

should be rapidly changed according to the input voltage [7]. To full this requirement, the ring oscillator design is modified by introducing buffer, shown in Fig 6, and it is designed using OTA in unity gain configuration as Fig 7.

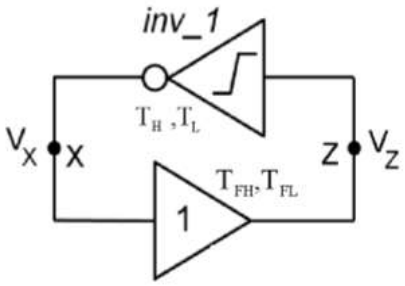

Fig 6: Equivalent topology of ring oscillator with buffer and inverter

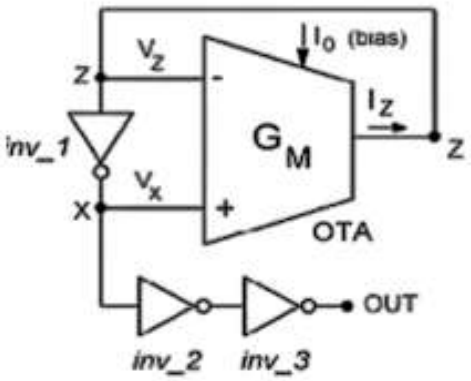

Fig 7: CCO using OTA

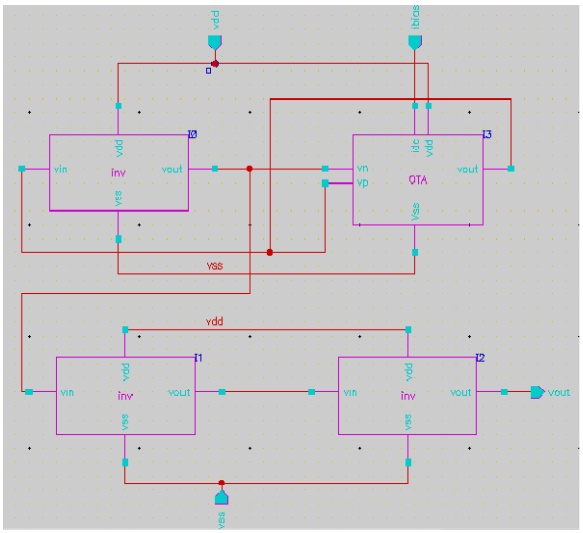

Fig 8: Schematic of CCO

4. *Voltage to Current Converter (V-I Converter)*

The V-I converter converts the V_{cntrl} to a proportional bias current I_{bias}. This output from the V-I converter is fed to the CCO and it act as the controlling current for CCO output frequency. The shown in Fig 9 takes the control voltage and converts it to a proportional bias current. The bias current is fed to the CCO, which generates an output frequency proportional to the bias current [3].

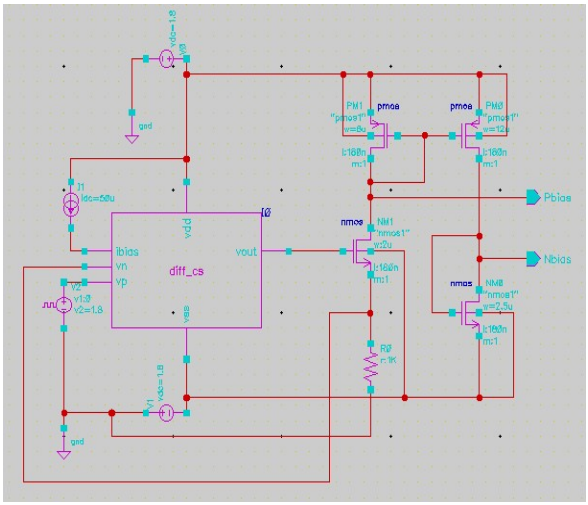

Fig 9: Voltage to Current converter using opamp

The current flowing through Q1 can be controlled by varying the gate voltage appalid to it. Mathematically,

$$I_x = \frac{V_c}{R_x} \qquad (1)$$

The cascaded circuits of two amplifier stages form the opamp circuit here. The first stage is The two stages of Opamp is used for amplification in two-stage configuration in which the first stage is a Differential Amplifier and second stage is implemented by employing a Common Source (CS) Amplifier. Fig 10. The CS amplifier has been used which is able to provide large gain in output stage [4].

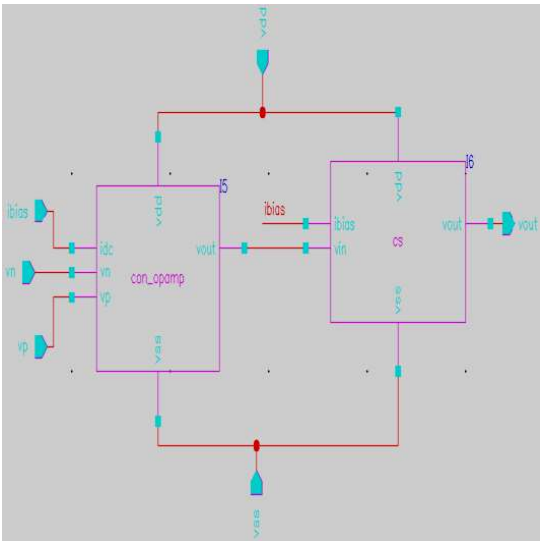

Fig 10: Schematic of cascaded CS and differential amplifier to form Opamp

IV. IMPLEMENTATION AND SIMULATION

Cadence Design Environment version IC 6.1.6. Virtuoso Schematic and Spectre is used for schematic design and its simulation and Layout XL for layout design.

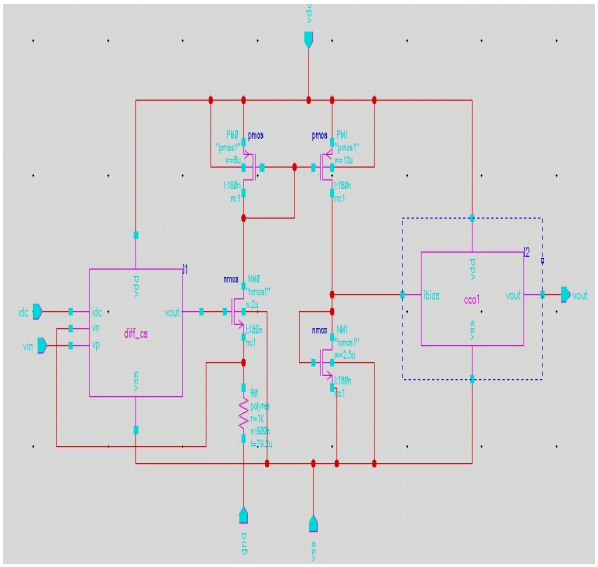

Fig 11: Schematic of VCO

Transient, DC and AC analysis is performed on individual blocks of the designed VCO

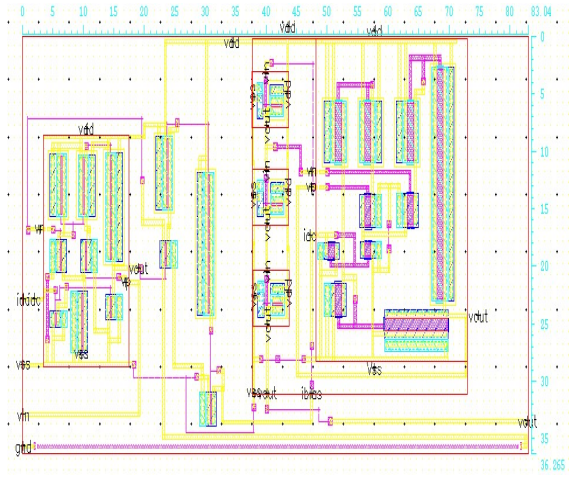

Fig 12: Layout of VCO

Layout area for VCO is found to be 2963.03μm^2. DRC and LVS simulations are performed.

V. RESULT ANALYSIS

Transient analysis is performed for analysing the working of Voltage to current converter. During analysis, it is observed that if sin or square waves are the input wave forms with an input voltage Vcntrl, the output wave form with corresponding wave form for output current , I_{out} is sine or square respectively as shown in Fig 13. This shows the linearity between I_{out} and V_{cntrl}. Thus the circuit designed works as a V-I converter.

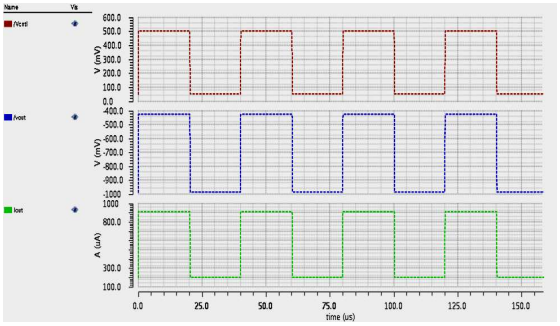

Fig 13: Transient analysis of voltage to current converter

Table 1 represents different values of I_{out} obtained for values of V_{cntrl}.

TABLE 1: I_{out} values for different values of V_{cntrl}

V_{cntrl}(mV)	I_{out}(uA)
5	11.3
10	38.55
30	115.2
50	180.1
100	320.3
200	575.6
300	810

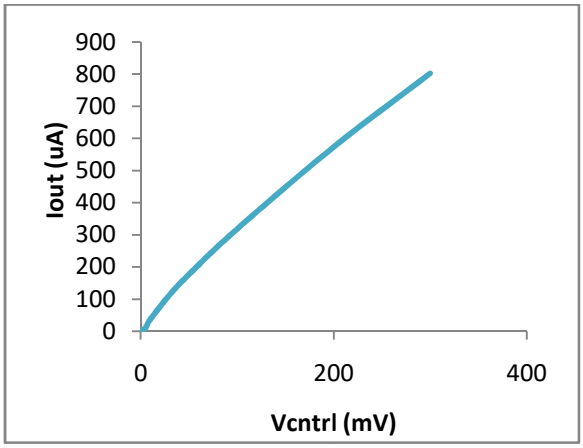

Fig 14: Plot of V_{cntrl} v/s I_{out}

The testing of OTA done with fixed bias current, varying the values of K and for fixed value of K, varying the bias current. It is observed that,

1. The I_{bias} and the gain and output resistance are inversely proportional
2. I_{bias} is directly proportional to f_{3dB} increases.
3. K and gain are inversely proportional. As K increases, gain decreases.
4. K and f_{3dB} are directly proportional. As k increases, f_{3dB} also increases. But but K cannot be increased to

a large value as it results in decrease of gain. K=8 is the maximum possible value to maintain the gain.

5. The output resistance and K are inversely proportional. As the value of K increases, output resistance decreases.

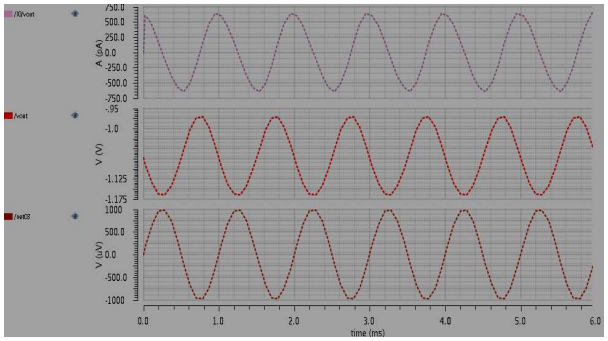

Fig 15: Transient analysis of OTA

Because of the capacitive load at OTA, the output current has a 90^0 phase shift with the input.

The stable phase margin for OTA must be above 60°. As the value of the phase margin increases, the OTA becomes more stable.

TABLE 2: Stability analysis of the OTA for different values of I_{bias}

I_{bias}(uA)	Phase Margin	Gain(dB)
30	121.265°	46.02
50	72.23°	45.89

From transient responce, it is observed that the output frequency is found to be changing for different input voltage (V_{cntrl}). Also the VCO operating frequency range is from 60MHz to 435MHz.

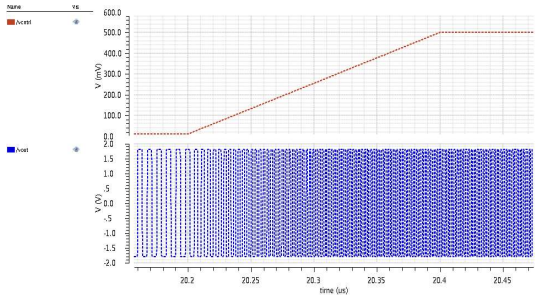

Fig 16: Transient response of VCO for different levels of V_{cntrl}

LVS and DRC simulations are performed and no errors are found. There for layout placement is according to the design standards and no mismatch is found in schematic and layout.

VI. CONCLUSION

Voltage Controlled Oscillator is one of the most power consuming unit in a PLL due to its rapid and continues operations. This paper focuses on a design of VCO with low power consumption for PLL. V-I converter and CCO are the main circuits in VCO. The V-I converter is implemented using a two staged opmap with differential amplifier as first stage and the cascaded CS amplifier as second stage.

The Current Controlled Oscillator consists of OTA and CMOS inverters. OTA is a combination of sinking current mirror, sourcing current mirror and differential pair. It is mandatory that the input and output nodes of these circuits should be at high impedance. The aspect ratio is selected to make the CMOS to work in saturation region. Since the value of scaling factor K effects the output gain inversely, it is taken as 4 which gave better values of output gain and 3dB frequencies.

Here the OTA and CMOS inverter required for the CCO are designed and simulated. The OTA and CMOS inverters are integrated to form a working CCO and various parameters of CCO has been analysed. Finally, the V-I converter and the CCO is integrated to form a VCO.

The VCO is tested with different values of V_{cntrl} values and it is observed that the output frequency changes with respect to the input voltage to the system.

TABLE 3: Comparison of parameters with the previous work[1][2]

Parameters	Previous work	This work
Operating frequency range (MHz)	640 - 800	60 – 435
Power consumed by VCO (mW)	24	7.31
Layout area of VCO (μm^2)	50000	3012.75
VDD (V)	1.8	1.8
Technology (nm)	180	180

REFERENCES

[1] Gauri Shankar Singh, Devesh Singh, S.Moorthi, "Low Power Low Jitter Phase Locked Loop for High Speed Clock Generation" in Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PRIMEASIA), December 5- 7 2012, pp. 192-196.

[2] H.Barthelemy, S.Meillere, S.Bourdel "Single ended rail-to-rail CMOS OTA based variable-frequency ring-oscillator" , IEEE conference on Circuits and System, May 2004, pp.537-540.

[3] Donald T. Comer, David J. Comer "A CMOS voltage to current converter for low voltage applications" in springer journal on Analog integrated circuits and signal processing, vol. 26, no. 2, pp 117-124, 2001.

[4] Adel S. Sedra, Kenneth C. Smith "Microelectronic circuits: Theory and applications", 6th International edition, Oxford University Press, 2011

[5] R. Jacob Baker "CMOS- Circuit Design, Layout and Simulation" 2nd edition, IEEE Press Series, Microelectronic systems.

[6] Olga J Antonova, Diana I Punkneva, Emil D Manolov, Marin H Hristov "Design of CMOS OTA core for practical education" IEEE 27th international Spring seminar on Electronics technology, vol.2, pp. 332-337, 2004.

[7] G.Jovanovic, M.Stojcev, Z.Stamenkovic "A CMOS Voltage Controlled Ring Oscillator with Improved Frequency Stability", Scientific publications of the State University of Novi Pazar ,vol. 2, no.1 pp.1-9, 2010

[8] Raja Sen, Arko Banerjee, Satyaki Banerjee, Sayanta Roy Chowdhury "Design of an Oscillator Using CMOS Operational Transconductance Amplifier (OTA)" International Journal of Electrical and Computing Engineering, vol. 1, no. 1, July 2014.