A Standard-basis Based CDMA NOC Design

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***Abstract*— NOC's has come into existence to resolve the problems in the conventional bus based on-chip communication. Earlier circuit switched and packet switched methods were employed in NOC's and recently CDMA based NOC's have gained popularity because of its capability of handling communication nodes concurrently. The CDMA technique is very handy in SOCs for establishing communication among a large number of integrated components on the same chip. The CDMA spreading codes for NOC such as Walsh codes were used for implementing the encoding/decoding part of CDMA and recently a new spreading code called Standard-basis Based (SB) was used in the encoding/Decoding process. In this paper, the CDMA NOC using the Walsh codes and SB codes are implemented individually on FPGA SPARTAN III kit. The design is coded in Verilog on Xilinx ISE and simulated using Modelsim 6.3f. The CDMA NOC SB and WB Coding designs are implemented on FPGA –Atrix7 and the performancesare compared. The implementation results of the two methods are compared.The designed SB code CDMA NOC has improved 30.11% area in LUT slices, 12% reduction in total power consumption and 4% faster.**

Keywords—Network on Chip; CDMA; Spreading code; FPGA;

I. INTRODUCTION

In SOC's the increase in the number of IP cores have made the traditional bus based on chip communication replaced by Network -on-chip to reduce the complexity and provide parallelism in communication between IP cores implemented in SOCs. NOC's provide a structure for providing communication between a large number of IP cores and other components on Chip. The NOC structures are of two types circuit-switched and packet-switch networks. In circuit- switch type, routing resources are allocated by the NOC to establish a link between the sender and the receiver.TDM and FDM are the two techniques used by the circuit switched NOC to share the bandwidth. The circuit switched NOC type suffer from complexity and contention problem for a large number of interconnected components such as found in SOC's. Packet switch NOC overcomes the shortfalls of circuit switched type allowing data packets use a shared link for communication, thereby eliminating contention problems. This type suffers from a large variation in packet transfer delays when using multi-hop point to point connection. To overcome this drawback, a CDMA technique has been utilized in NOC.

Traditionally CDMA was known to be one of the popular wireless communication multiple access techniques, but now CDMA is employed in wired communication primarily to provide on-chip communication. The CDMA technology uses encoding/decoding procedure to transfer data from different users simultaneously. The data is multiplied with a spreading code at the sender side to get encoded data and such encoded data from different users are sent simultaneously over a common link. The received data is multiplied with the spreading code at the receiver end. The above principle can be made use of in NOC to provide on-chip communication however the spreading code used in NOC are different to that used in wireless communication.An important feature of spreading codes is it possesses orthogonal and balance properties. Codes being Orthogonal refers to the autocorrelation of codes should be one while the cross-correlation should be zero which aids in sending different data on different code without any interference. Balance property refers to the code having an equal number of ones and zeros. These properties make the CDMA method less prone to noise and interferences.

The CDMA NOC architecture which uses "Walsh codes" is described in [4]. An 8 bit Walsh code encoding procedure was shown in [2].For a Walsh code of X bits, X-1 simultaneous communication is possible. A CDMA NOC based on standard–basis (SB), encoding/decoding method, is proposed in [7].

In this paper, a performance evaluation of the Walsh codes and the SB codes is performed. An NOC based on Walsh codes is designed and implemented on FPGA and similarly, the SB code is implemented. A comparison of the implementation parameters such as Area and Power is done.

The paper is organized as follows Section II discusses the Background of CDMA in NOC Section 3 discusses the review of literature Section IV presents the Implementation Section V is the Results section while Section VI is the Conclusion.

II. OVERVIEW

A) CDMA NOC Structure

The CDMA NOC is a packet switched communication NOC which uses spreading CDMA codes. The architecture FOR CDMA NOC consists of

1) Network-Node
2) Transmitter module
3) Network-Arbiter module

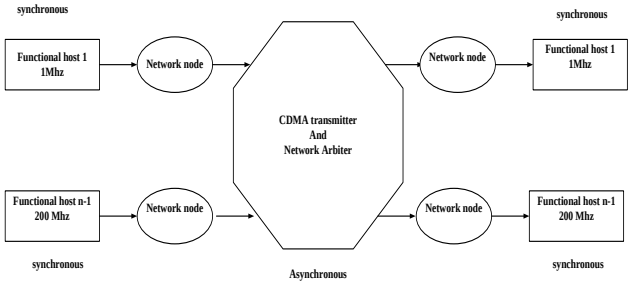

Figure1shows the structure of CDMA NOC

The functional hosts represent the IP cores which require communication. Each host can send its data to the CDMA switch through the Network Nodes. The sending data is framed along with Destination Address (DA) as a packet in the Network node. The packet to be transmitted will be encoded using suitable spreading codes and transmitted to the destination using Network Arbiter and a transmitter. If the functional hosts send data at different data rates, then a "Globally Asynchronous and Locally Synchronous" kind of mechanism are used where the communication between the functional host and N/w node is made synchronous while the communication among the network nodes through the CDMA switch is asynchronous.

1. Network-Node:

The network node accepts the data sent from the functional host using synchronous communication. The data will be framed as a packet including the DA. The packet will then be forwarded to the CDMA transmitter. The subcomponents of Network Node are

- Node-IF
- Transmitter Packet Buffer
- Receiver Packet Buffer
- Packet-Sender
- Packet-Receiver

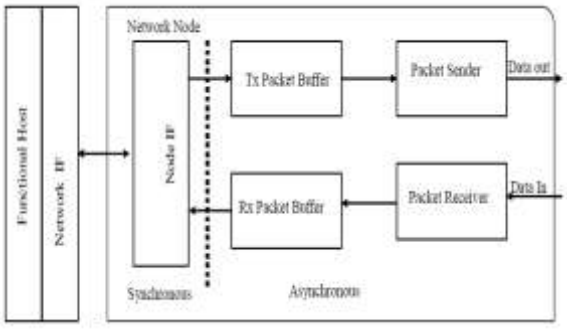

Figure 2 shows the structure of Network-Node

i. *Node-IF:* This sub-block provides an interface between the functional hosts and the network node.This subblockcollects data from functional-host and forms a packet. The collected packetis shifted to transmitter packet memory of Network-Node. This sub-module receives the data through receiver packet memory disassembles the packet and forward the data to the functional host.

ii. *TX packet buffer:* This submodule is a buffer for storing the incoming packets from Node-IF and shift it to packet sender sub-block.

iii. *RX packet buffer:* The function of this sub-module is to deliver the data packets from packet receiver to Node-IF.

iv. *Packet Sender:* This submodule first finds whether the TX Packet Buffer block is non-empty. If it is non-empty, the packet sender fetches the data from TX buffer, extracts the destination address and forwards it to the Network Arbiter. It sends the data to CDMA TX until Network receives the grant signal.

v. *Packet-Receiver:* This submodule waits for NA to select a spreading code. Once the spreading code is known, this module will decode the data from the CDMA TX and forward it to RX packet buffer.

2. Network-Arbiter module:

This module sets up the channel to transfer data for the sender & receiver. This block mainly resolves the contention for data transfer. The Packet RX block is capable of receiving data from a single user, and if many senders try to send their data to the same destination, contention arises and the NA is used to solve such issues using Round Robin arbitration or FCFS scheme. In origin of the process, if a Network Node possesses any data to send to other destination nodes, then Destination-Address is first sent to theNA module. The NA module first informs the receiver node related to data transfer, if the receiver node responds with the signal to the NA, then it will issue a grant signal to the sender node permitting it for transmission.

3. Transmitter-Module

The transmitter module receives the data from the sender node and uses a spreading code to encode the data. The module performs this encoding process independently for every data sent from a different node. The module uses a bit-synchronous scheme of data transfer. To understand bit synchronous scheme, consider three packets P1, P2, P3. P1 and P2 arrive at the transmitter at the same time while P3 arrive late. The data bits of P1 will be encoded parallelly and transferred simultaneously in synchronous with the data bits of P2. The starting data bits of packet c will be handled along with the next bits of P1 and P2. This bit-synchronous scheme avoids interference resulting from phase offsets in spreading codes when they are transmitted asynchronously.

B) SB Encoding & Decoding

In the SB scheme, the encoded data E is generated by I and C in chip manner with an AND operation

$$E_1^i = I_j^i \,.\, C_j^i \qquad \ldots\ldots.1$$

The sum data is expressed as

$$S_j^i = E_1^i \;\; XOR \;\; E_2^i XOR \, E_3^i \qquad \ldots\ldots.2$$

$I_j \rightarrow$ *The value of the original bit of sender* j
$I_j^i \rightarrow$ *The logical value of ith chip in* I_j
$E_j \rightarrow$ *The encoded data chips of sender* j
$E_j^i \rightarrow$ *The logical value of ith chip in* E_j
$C_j \rightarrow$ *The orthogonal coder to sender* j
$C_j^i \rightarrow$ *The logical value of ith chip in* C_j
$S \rightarrow$ *The sum of data chips generated by encoder*
$S^i \rightarrow$ *The logical value of ith chip in* S
$D_j \rightarrow$ *Data extracted from* S^i *by AND gate in receiver* j
$D_j^i \rightarrow$ *The logical value of ith chip in* D_j

Table 1 explains the notations

The encoding process is shown using the waveform

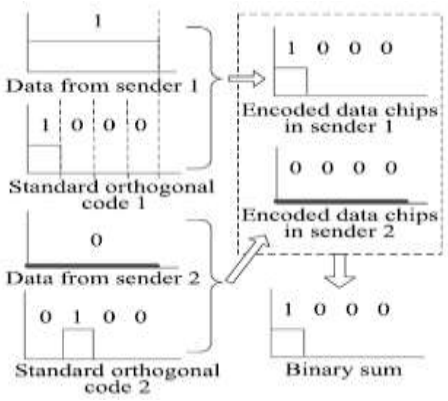

Figure 3 shows the structure of CDMA NOC

The decoding process is expressed as

$$D_1^i = S^i \ . C_j^i \qquad \ldots\ldots 3$$

The output bit in receiver j is expressed as

$$Y_l = \sum_{i=1}^{m} D_i^i \qquad \ldots\ldots 4$$

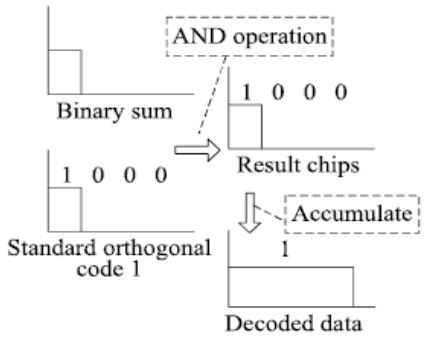

Figure 4 shows the structure of CDMA NOC

III. REVIEW OF LITERATURE

This section discusses the various NOC architectures along with the spreading codes used.

S.Shimizu et al. [3] proposed a Parallel bus system which uses CDMA technology. In the parallel bus interface, one-bit data can transfer from transmitter to receiver in a single clock along with great noise tolerance. The Parallel CDMA bus-structure contains three important modules; Transmitters, Receivers, and Stabilizer. The multiplication of the data with PN sequence is achieved using wiring method to reduce the number of logic gates and delay. The stabilizer will add all the signals from the transmitter using a capacitor coupling circuit along with the refresh management circuitry. The receivers multiply the incoming encoded data with PN sequence using a wiring method. Differential amplifiers are used to collect the data from the multipliers.The P-CDMA architecture using PN sequence codes showed high transfer timing tolerance with high noise-tolerance.

A CDMA NOC architecture which uses “Walsh codes” as the spreading code is discussed in Kim et al. [4]. An architecture of the CDMA switch / local switch which could handle communication among seven network nodes was illustrated.The architecture used 8-bit Walsh code generator which generates seven non-zero Walsh code words, each uniquely assigned to seven network nodes/sources connected to the switch. FIFO buffer was used for store and forwarding facility and schedulers were used for avoiding contention problems. The TX block selects Walsh codes associated with the destination and modulates the data bits with the spreading codes. An adder block in the architecture adds all the seven code words from the TX block and sends it to the RX blocks. The data forwarded to the respective RX is extracted using their appropriate spreading Walsh codes. A hierarchical Network Switch can be constructed using the proposed local switch architecture. The authors showed the construction of star based hierarchical structure. In this architecture, if a source has to send data to the destination in other local switch areas, the data packet travels through central-switch. Therefore all local switches are interconnected with the main central switch in a regular order. Hence there are seven local-switches which are interconnected with central switch in two-level star network topology.

The authors X.Wang and J.Nurmi [5] developed a CDMA NOC architecture to avoid the latency problems found in P2P Packet-switch on-chip communication n/w. The NOC was modeled and implemented on Register Transfer Level using (VHSIC) hardware description language. The architecture supported GALS (Globally Asynchronous and Locally Synchronous) scheme of transfers to include both synchronous and asynchronous circuits. Spreading code policy was employed which provides information on how the codes can be used. The proposed CDMA NOC architecture used A-T protocol to reduce complexity in decoding. A Network node acting as an interface to the source was developed in the architecture. For the simulation purpose, a 6-node CDMA-network was constructed. It was verified that data could be transmitted parallelly in time-domain through CDMA NOC architecture. The proposed architecture outperformed the point to point packet switched on-chip communication network.

The use of Standard-basis Based CDMA in NOC was presented by Wang et al. [base paper].The SB codes were used to overcome the drawbacks of design complexity and Low code utilization observed in Walsh codes. The authors propose a new architecture wherein the data from the sender programmable elements (PE) are converted to serial using P2S. The serial data is then coded using SB encoders. The codes from all encoders are added in an Adder block and then the resulting sum data is transmitted. The receiver uses their SB codes to decode their data from the sum signal. The serial data bits are parallelized using S2P and sent to the destination PE.

IV. SYSTEM DESIGN

The section discusses the design of CDMA NOC with SB codes using a block diagram shown below.

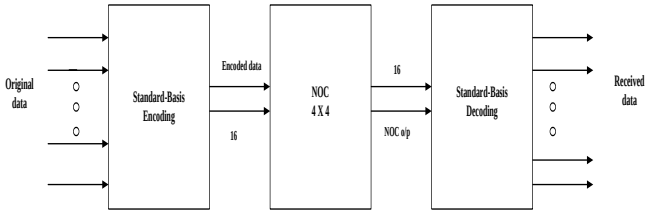

Figure 5 shows the design of CDMA NOC with SB codes

The CDMA NOC design is implemented with SB Encoding block, a mesh routing n/w and an SB decoding block.

Steps:

1. The incoming serial single bit data is encoded with n=16-chip SB code in the SB encoder.
2. With m=16, 16 different serial single bit data is encoded and summed.
3. A 4x4 mesh topology n/w transfers the encoded data to the decoder side.
4. Based on the (X-Y) routing algorithm the packets are routed to the decoder block.
5. The decoder takes the encoded data from the n/w decodes it and provides 16 different single bit data.

The Standard-basis Based Encoder circuit using n-chip SB code and m different single bit data. The data bit is ANDED with n bit SB code to get SB encoded n chips. A sum signal is generated by performing XOR operation on the encoded data from other senders.

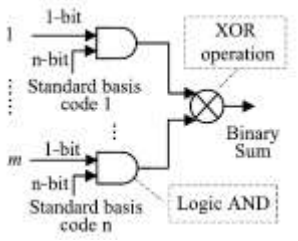

Figure 6 shows the SB encoder design

Standard basis Based Decoder circuit which outputs single bit decoded data using SB codes. The logical AND operation is performed for SB code and the arrived sum-bits. The resultant chips are accumulated to form a single bit in the accumulator.

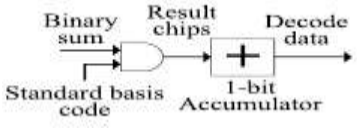

Figure 7 shows SB decoder design

The implementation of CDMA NOC using Walsh code is shown below.

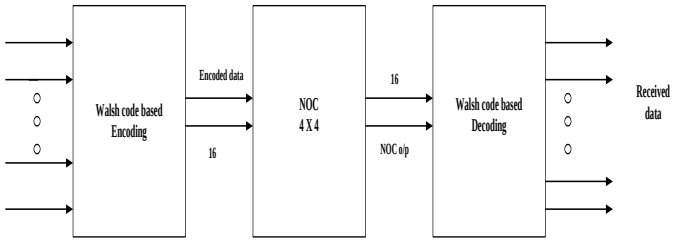

Figure8 shows the structure of CDMA NOC using Walsh codes

The Walsh code-Based Encoder circuit using Walsh codes of length n and m such different serial single bit data. The single data bit is encoded using a Xor operation and m such encoded data is added to form a multi-bit sum signal.

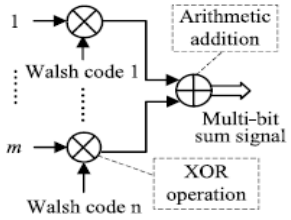

Figure 9 shows the structure Walsh Encoder

The Walshcode-Based Decoder circuit uses two accumulators to store the value of data from the incoming chips. The received sum bits is placed in positive accumulator part if chip value is 0 or placed in negative part accumulator if chip value is 1. The two accumulator data are compared if positive accumulator part is greater then decoded data bit is 1 else 0.

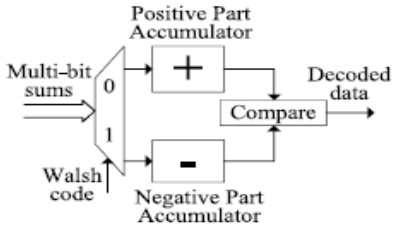

Figure 10 shows the structure of Walsh Decoder

The NOC Routing architecture is implemented

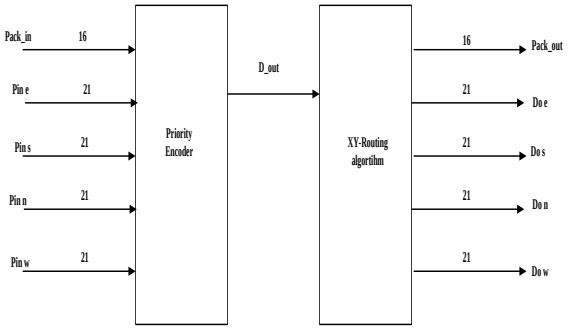

Figure 11shows the structure of Router Node

The Encoder contains 5-inputs shown in below figure. Inputs are pack_in, and from East, South, North, West side of the processing node.The outputs are connected with cross bar switch and this switch will connect the packet into the corresponding node using an X-Y routing algorithm.

V. RESULTS

CDMA NOC Using SB Coding Method Results

a) SB Encoding Module Results

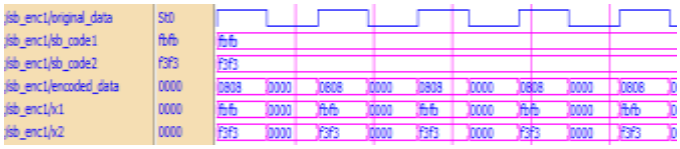

Figure 12 SB Encoding Method Simulation Results

b) SB Decoding Module Results

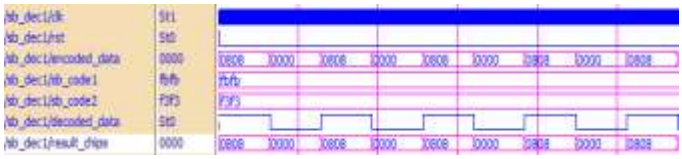

Figure 13 SB Decoding Method Simulation Results

c) WB Encoding Module Results

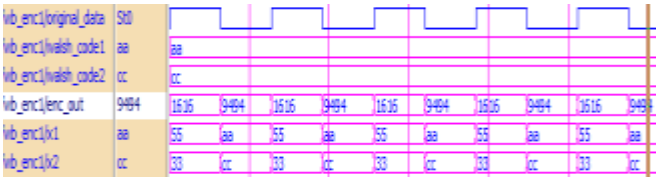

Figure 14 WB Encoding Method Simulation Results

d) WB Decoding Module Results

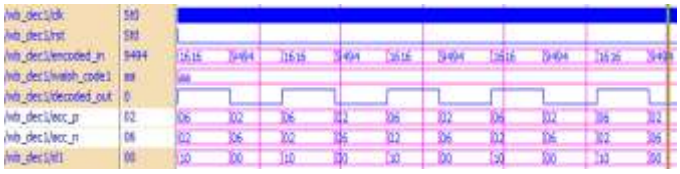

Figure 15 WB Decoding Method Simulation Results

e) Router Single Node Module Results

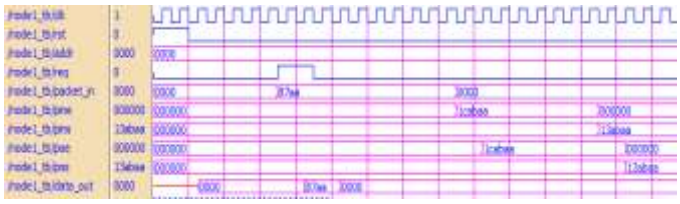

Figure 16 Router Single Node Module Simulation Results

f) PERFORMANCE ANALYSIS

The Comparison of CDMA NOC SB and WB methods with respect Area, Power and timing delays are shown.

Area comparison: The areas used regarding Slices, LUT are shown below for both SB and WB techniques.

Device:Artix7 7A100TCSF324		**CDMA NOC SB CODING**		**CDMA NOC WB CODING**	
Resource used	**Available**	**used**	**utilization**	**used**	**utilization**
Number of Slice Registers	126800	1543	1%	1536	1%
Number of Slice LUTs	63200	2043	3%	2926	4%
Number of bonded IOBs	210	146	69%	130	61%
Number of BUFG/BUFGCTRLs	32	1	1%	1	1%

Table 2 Comparison analysis of CDMA NOC SB and WB Coding – AREA

The slice LUT's are improved around 30.11% in SB Coding compared to WB Coding. It reduces the hardware complexity of the CDMA NOC systems.

*Timing Analysis:*The Timing summary and its Comparison analysis of CDMA NOC SB and WB Coding are shown in The SB Coding design speed up around 33.13% than WB Coding.

Timing analysis	**SB Coding**	**WB coding**
Minimum period	1.947ns	2.012ns
Maximum Frequency	513.505MHz	496.969MHz
Setup time	1.806ns	1.954ns
Hold time	0.640ns	5.684ns

Table 3 Comparison analysis of CDMA NOC SB and WB Coding – TIMING

The Clock-Frequency is similar to Chip-Frequency and set as 2.5 GHz. The power analysis of CDMA NOC SB and WB Coding are shown in Table 5.9©. In total power and dynamic power of SB Coding is improved around 12% and 13.11 % than WB Coding.

Power analysis

Power analysis	**SB Coding**	**WB coding**
Total power	0.750W	0.852W
Dynamic Power	0.666W	0.767W

Table 4 Comparison analysis of CDMA NOC SB and WB Coding - POWER

Throughput calculation:

SB CODING = (Maximum frequency /latency)* Number of Input bits.

= (513.50MHz /2)/ 16 = 4.104 Gbps

WB CODING = (Maximum frequency /latency)* Number of Input bits.

= (496.96MHz /2)/ 16 = 3.975 Gbps

VI. CONCLUSION AND FUTURE WORK

The CDMA Encoding / Decoding methods for on-chip communications is designed and implemented. The Standard-basis (SB) based and Walsh–Code (WB) Based encoding and

decoding are designed for CDMA NOC's. The two CDMA NOC are designed the first SB Encoding/decoding & NOC Router design which is mesh topology based and second one is WB Encoding/decoding & NOC Router Design. Our NOC Router design includes 16 nodes; the node works according to the XY-routing algorithm. The design is coded in Verilog on Xilinx ISE and simulated using Modelsim 6.3f. The CDMA NOC SB/WB Coding designs are implemented on FPGA – Atrix7 and physically verified.The performance parameters of SB coding are better compared to WB Coding. The slice LUT's of SB coding are improved around 30.11% than WB Coding. The maximum frequency of SB Coding design is increased around 33.13% than WB Coding. In total power and dynamic power of SB Coding is improved around 12% and 13.11 % than WB Coding. The throughput of SB coding is around 4% faster than the WB Coding.Overall there is an improvement in the area, timing, Total power,reduced hardware complexity andimproved Throughput of the SB Coding on WB Coding and

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