Test Architecture Optimization for 3-D Stacked ICS with Firm Dies

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Abstract: The semiconductor industry is pushing relentlessly for high-performance and low-power chips. Recent advances in semiconductor manufacturing technology have enabled the creation of complete systems with direct stacking and bonding of die-on-die. These system chips are commonly referred to as 3-D stacked ICs (SICs). Through-silicon via (TSV)-based 3-D stacked ICs (SICs) are becoming increasingly important in the semiconductor industry. In this paper, we will try to address test architecture optimization for 3-D stacked ICs implemented using TSVs. We consider the case, namely 3-D SICs with firm die test architectures that are still need to be designed. Here we have to propose the solutions to achieve significant reduction in test length. This will be achieved through proposed test architecture and also to reduce the width of the Test Access Mechanism (TAM) by using serial/parallel conversion technique. Using TSV technology, 3-D ICs are created by placing multiple device layers together through wafer or die stacking, and these are then connected using vertical TSVs.

Keywords: 3-D stacked ICs, Through-silicon via (TSV), Test Access Mechanism (TAM)

I. INTRODUCTION

The semiconductor industry is pushing relentlessly for high-performance and low-power chips. Recent advances in semiconductor manufacturing technology have enabled the creation of complete systems with direct stacking and bonding of die-on-die. These system chips are commonly referred to as 3-D stacked ICs (SICs). Through-silicon via (TSV)-based 3-D stacked ICs (SICs) are becoming increasingly important in the semiconductor industry. In this paper, we will try to address test architecture optimization for 3-D stacked ICs implemented using TSVs. We consider the case, namely 3-D SICs with firm die test architectures that are still need to be designed. We next present the objective to derive optimal solutions for the architecture optimization problem for the above mentioned case. Here we have to propose the solutions to achieve significant reduction in test length. This will be achieved through proposed test architecture and also to reduce the width of the Test Access Mechanism (TAM) by using serial/parallel conversion technique. Using TSV technology, 3-D ICs are created by placing multiple device layers together through wafer or die stacking, and these are then connected using vertical TSVs[8]. Testing core-based dies in 3-D SICs brings forward new challenges. In order to test the dies and associated cores, a Test Access Mechanism (TAM) must be included on the dies to transport test data to the cores, and a 3-D TAM is needed to transfer test data to the dies from the stack input/output pins[7][13]. Test-access mechanisms (TAMs) facilitate the modular testing of embedded cores in a core-based system-on-chip (SOC). Such a modular testing approach can also be used for emerging three-dimensional integrated circuits based on through-silicon vias (TSVs).

Core-based SOCs based on 3D IC technology are being advocated as a means to continue technology scaling and overcome interconnect-related bottlenecks. Embedded cores are now common-place in large system-on-a-chip (SOC) designs. However, since embedded cores are not directly accessible via chip inputs and outputs, special access mechanisms are required to test them at the system level. Test-access architecture, also referred to as a test access mechanism (TAM), provides the means for on-chip test data transport.

II. PROPOSED FIRM DIE ARCHITECTURE

In this section we proposed a distinguished architecture of overall test length as well as TAM optimization using serial-parallel conversion mechanism.

Figure 1: Proposed architecture of test length optimization using serial/parallel conversion hardware
III. PROPOSED ALGORITHM

Here we consider the architecture for 3-D SIC with firm die. In the case of firm dies, the test architecture for each die is pre-defined as for a hard die, but additional serial/parallel conversion hardware may be added to the die to allow for fewer test elevators (or test pins in the case of the lowest die) to be used than the fixed 2-D TAM width for the die. The conversion hardware is added before the inputs and after the outputs of the die wrapper. The input hardware multiplexes a smaller number of TAM wires to a larger number of die wrapper wires. Demultiplexers at the output of the die wrapper transfer test responses from a larger number of die wrapper wires to a smaller number of TAM wires. Compared to the scenario involving hard dies, this scenario allows the use of fewer test pins at the expense of higher test lengths, but it also allows additional flexibility in test scheduling and testing-time optimization.

Input : Total no. of dies(K;K=1,2,3,4,5), Tam requirement for each die(twm), tam requirement for Die 1(tw1), Associated Testing time for each die(tm), Maximum Available TAM Width(Wmax), Maximum Available TSVs(tsv_max), Test pins at Bottom Die(no_of_testpins)

Output: Optimal TAM schedule to minimize total testing time(Total_Testing_Time)

Step 1: Begin
Step 2: Set the dies with respect to test time
Step 3: Set the bottom die on the available test pins
Step 4: Testing Time T=0;
Step 5: if Wmax >= no of testpins then
   Display: remain tam;
   while K! = null do
   if tw1 <= Wmax then
      check=tsv_max(K);
   if check==TRUE then
      Allocate available TAM to K dies & Test;
      Schedule as parallel of K dies;
      t1=max(tm) among all dies in K ;
   end
   else
      Set Serial/Parallel Conversion=S_P_Convert (twm) Hardware;
      Allocate available Tam through serial/parallel conversion hardware to K dies & Test;
   end
   else
      Display: Testing is not possible;
   end
   if \( \sum twm \leq Wmax \) then
      Find all the combinations of dies from K ;
      Let S is a combination of dies such that \( \sum twm \) is maximum; check=tsv_max(S);
      if check==TRUE then
         Assign dies as parallel schedule;
         t1=max(tm) among all dies in S ;
      end
      else
         No combination of dies is found with maximum \( \sum twm \); end
      else
         Test the next combination as serial;
         t=t+t1 ;
      end
      K= K-1;
   end
   Set Total_Testing_Time(T)= T+t;
   Display:Total Testing Time;
   end
Step 6: else
   Display:Testing is not possible ;
   end
Step 7: End.
Algorithm: Proposed Test Scheduling Algorithm to Test Firm Dies

IV. CONCLUSION

Here we are considering the problem of test-architecture optimization for 3-D stacked ICs with firm dies. In the case of firm dies, the test architecture for each die is predefined, only serial/parallel conversion is allowed and we are trying to design the architecture with minimum number of TAM for each die to optimize the test length of the whole architecture and try to test maximum number of dies parallely with respect to serial testing using serial/parallel conversion technology. So, here we are determining an optimal TAM design with possible serial/parallel conversion widths for each die.

REFERENCE

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