PWM Based Inverter using Spartan 6 FPGA

Mahesh K. Patil[1], Vinod B. Kumbhar[2], Aditya N. Hambar[3], Girish S. Hasure[4]

[1, 2]*Asst. Prof, Dept of Electronics, DKTES's Textile & Engineering Institute, Ichalkaranji, Maharashtra, India*

[3]*Software Engineer, Global Edge Software Ltd, Bengaluru, Karnataka, India*

[4]*Project Engineer, Cerium Systems Pvt. Ltd, Bengaluru, Karnataka, India*

***Abstract*–In this paper, two pulse width modulated outputs are produced using the Spartan 6 FPGA ANVYL board. The first output signal contains one pulse in 0^0 to 180^0 and the second output signal contains same pulse as first output but shifted by 180^0 i.e. in 180^0 to 360^0. The width these signal is changed using control inputs. This PWM output signal is used as control input to the inverter circuit. The power at the load connected to the inverter is observed by changing the widths of the PWM outputs.**

***Keywords*- PWM, FPGA, ANVYL, ASIC**

I. INTRODUCTION

Pulse width modulation techniques have been intensively researched in the past few years. Methods, of various concept and performance, have been developed and described. Their design implementation depends on application type, power level, semiconductor devices used in the power converter, performance and cost criteria, all determining the PWM method. Two classes of PWM techniques have been identified: optimal PWM and carrier PWM. The optimal PWM technique for producing switching pattern is based on the optimization of specific performance criteria. In this case, the switching patterns are calculated a priorifor given operating conditions and are then stored in memory (look-up tables) for use in real time. In this project two PWM outputs are generated. The first output signal contains one pulse in 0 to 180 degree and the second output signal will contain same pulse as first output but shifted by 180 degrees i.e. in 180 to 360 degree. The width of those can be changed using control inputs.FPGA is a Programmable Logic Device (PLD), comprising thousands of logic gates. Some of them are combined to form a configurable logic block (CLB). A CLB simplifies high-level circuit design. SRAM or ROM defines software interconnections between logic gates, providing flexible modification of the designed circuit, without altering the hardware. Concurrent operation, less hardware, easy and fast circuit modification, comparatively low cost for complex circuitry and rapid prototyping make it the favorite choice for prototyping an Application Specific Integrated Circuit (ASIC).

II. SYSTEM BLOCK DIAGRAM

Fig.1 shows the block diagram of the entire system. The power at the load connected to the inverter is observed by changing the widths of the PWM outputs. This PWM output signal is produced by the FPGA based inverter. FPGA based inverter works as a controller circuit for inverter. Bulb or Lamp of 6V is used as a load. By varying the PWM output the intensity of the load (Bulb) can be changed. Spartan 6 FPGA Kit (ANVYL board) is used for generation of PWM output. Two Opto-couplers (TLP 250) and Two MOSFETS (2N7000) are used for making inverter circuit. Two 9V DC batteries are used as power supply this entire circuit.

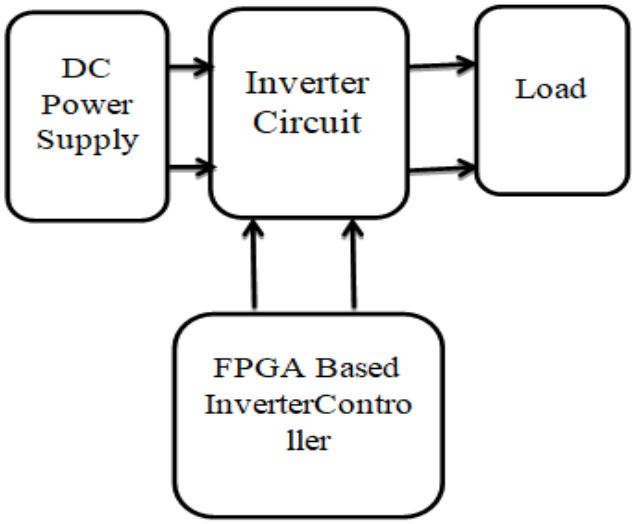

Fig.1 Entire System Block Diagram

Fig.2 shows the controller circuit for inverter using FPGA. It produces two PWM outputs. This program is written in VHDL language. CLK- is the input clock signal for counting the time period. CNT- is two bit input signal. According to the combinations of these bits the PWM width will change.

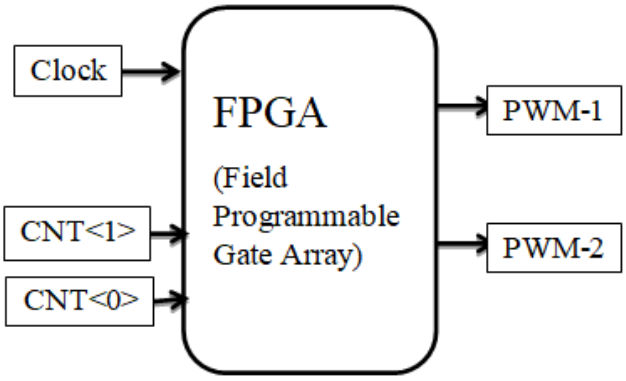

Fig.2 Controller circuit for inverter using FPGA

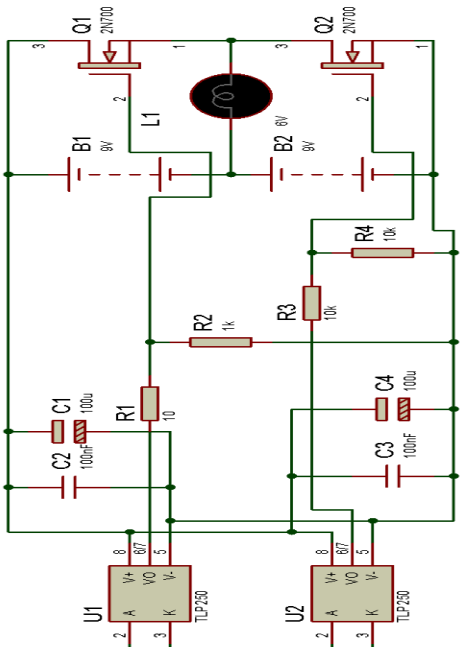

Fig.3 Detailed Circuit Diagram of system

III. WORKING OF SYSTEM

In the program, there is a variable declared is T which is used for defining the period of the PWM wave. In order to produce a PWM wave, there is one process having sensitivity on CLK signal. This means whenever there is a change in CLK signal i.e. every rising edge of clock this process will execute. In this process, the value of T starts incrementing with every rising edge of clock. If the value of T is greater than the predetermined value, then value of T will be 1 and it starts incrementing with CLK. The predetermined value is already defined in the program. It depends upon required frequency of the output. If we want to change the frequency, then it is necessary to change that value in program. Another variable defined is W which corresponds to the width of PWM wave.If the value of T changes then according to that the PWM wave will generate by another process. PWM1 is present in half portion of total time period and PWM2 is present in next half portion of time period. According to the combination of CNT bits, the width of the PWM will change. Thus the outputs of this program are two PWM signals whose widths will vary manually by selecting the combination of CNT bits.

Above mentioned PWM waves are given to the two opto-couplers. Opto-couplers are used to isolate the FPGA and driver circuit. The half wave bridge inverter circuit is used as a driver circuit. Switching devices in the driver circuit are two MOSFETs. The outputs of opto-couplers are given to the base of the MOSFETs. When the first PWM wave is high, first MOSFET will turn ON. Similarly, when the second PWM wave is high, second MOSFET will turn ON. There is no possibility of turning ON two MOSFETs simultaneously. For second condition the current flowing through the load is reverse with respect to the current flowing in first condition. Thus we get the alternating quantity at the load.

IV. EXPERIMENAL RESULTS

Frequency	CNT= '00'	CNT= '01'	CNT= '10'	CNT= '11'
50 Hz	1.51 V	1.84 V	2.31 V	2.83 V
500 Hz	1.03 V	1.58 V	2.16 V	2.63 V
5 kHz	0.5 V	0.8 V	1.25 V	1.9 V
50 kHz	0.78 V	1.16 V	1.54 V	2.1 V
500 kHz	0.1 V	0.18 V	0.29 V	0.4 V

TABLE 1 Load Output Voltage for different CNT and CLK frequency

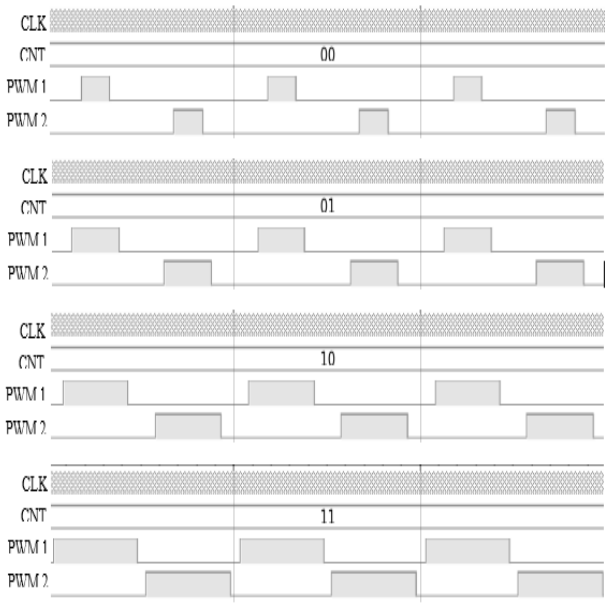

Fig.3 PWM1 & PWM2 outputs for different CNT, CLK

IV. CONCLUSION

As seen from above results, it is cleared that when the width of the PWM wave increases the voltage across the load increases. Thus the intensity of the bulb which is used as a load is increases. But it is also seen from the results that when the frequency of the output PWM wave increases the output voltage decreases. Thus the intensity also decreases. The reason is the switching time of the switching device used in the half bridge inverter (here MOSFETs are used). Because of this the average output voltage across the load decreases. This results in the decrease in intensity of load. Another parameter is the signal integrity. At the frequency ranging from 100 Hz to 500 kHz the output signal is pure in form. There is no any distortion in amplitude. But in case of lower frequencies (less than 100 Hz) the output wave is amplitude distorted. Noise present is very high. Thus the output is flickering and thus there is no constant output at all. In case of higher frequencies (higher than 500 kHz) the output voltage is very less.

V. FUTURE SCOPE AND APPLICATION

Such design of PWM generation can be used for a very fine control for switching circuits like inverter, power filters etc. By applying such digital PWM signal generation technique to Inverter circuits we can change not only voltage but also frequency and phase of the signal. For generating both one phase and three phase supply we can use this type of digital design.

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