Reduced Switches Multi Level Inverter

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Abstract: **Now a days a Multilevel inverter topologies are used as static VAR compensators, high voltage grid interconnections and variable speed motor drives. The Multilevel inverter performance is high compared to the conventional two level inverters due to their reduced harmonic distortion and less amount electromagnetic interference. In this scenario, Cascaded H Bridge MLI is preferred and the performance of the inverter can be improved by using different pulse width modulation techniques. The main disadvantage of the Cascaded MLI is complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. So in order to overcome the complexity nature the reduced switches multi-level inverters are proposed in this paper. So that the topology and the proposed topology multi-level inverters are compared with the Cascaded H bridge MLI. These methods are modeled by using the MATLAB/SIMULINK and the THD of these inverters are compared.**

Index Terms **- cascade inverter, multilevel, PWM, and THD.**

I. INTRODUCTION

The voltage source inverters produce an output voltage or current with levels either 0 or ±Vdc. They are known as the two- level inverter. To produce a quality output voltage or a current wave form with less amount of ripple content, they require high switching frequency. In high- power and high voltage applications these two level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings. These limitations can be overcome using multilevel inverters. There are 3 types of multilevel inverters named as diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter. These three types of multilevel inverters require more no. of components such as switches, clamping diodes and capacitors. As the number of voltage levels m grows the number of active switches increases according to 2×(m-1**)** for the cascaded H-bridge multilevel inverters. Multilevel inversion is a power conversion strategy in which the output voltage is obtained in steps thus bringing the output closer to a sine wave and reduces the total harmonic distortion (THD).

II. CASCADED H-BRIDGE INVERTER

The cascade H-bridge inverter is a cascade of H-bridges, or H-bridges in a series configuration. A single H-bridge inverter is shown in fig (1) and three phase cascaded H-bridge inverter for seven-level inverter is shown in fig (2). Fig (1) and fig (2) shows the basic power circuit of single H-bridge inverter and the cascade of H- bridge inverter for seven-level inverter respectively. An N level Cascaded H bridge inverter consists of series connected (N-1)/2 number of cells in each phase. Each cell consists of single phase H bridge inverter with separate dc source. There are four active devices in each cell and can produce three levels 0, Vdc/2 and –Vdc/2. Higher voltage levels can be obtained by connecting these cells in cascade and the phase voltage Van is the sum of voltages of individual cells,

Van = V1 + V2 + V3 + :::: + Vn.

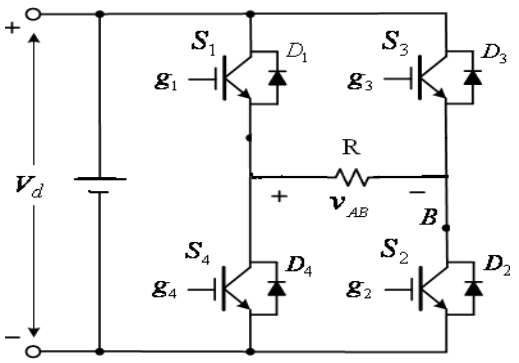

Fig.1 Configuration of single-phase H- bridge inverter

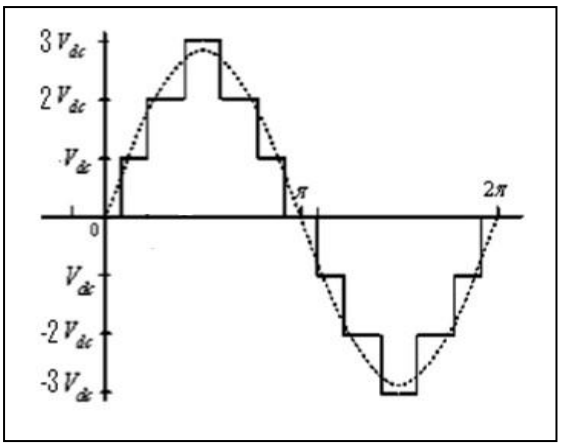

Fig.2 Configuration of three-phase

Cascaded Seven Level H-Bridge Inverter A three-phase CMI topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage waveforms and offers the potential for AC system phase- balancing. A series of single-

phase full bridges makes up a phase for the inverter.

For real power conversions, (ac to dc and dc to ac), the cascaded-inverter needs separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic, and biomass, etc.

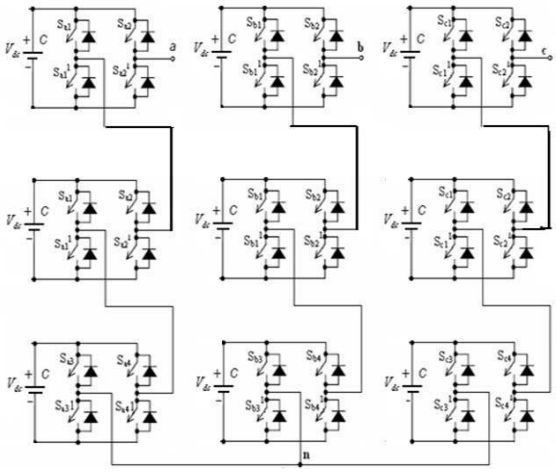

Fig.3 Output wave form of single phase 7 level cascaded inverter

The output wave form of the seven level inverter is shown in the fig.3.As the amount of levels increases in the inverter there is a possibility of the occurrence of the sinusoidal output. The multi-level output is more accurate and as the number of levels increases the smooth waveform

III. MODULATION TECHNIQUES

There are different control techniques available for a CHB MLI [13, 15]. Among all those techniques, PWM control technique which produces less total harmonic distortion (THD) values is most preferable.

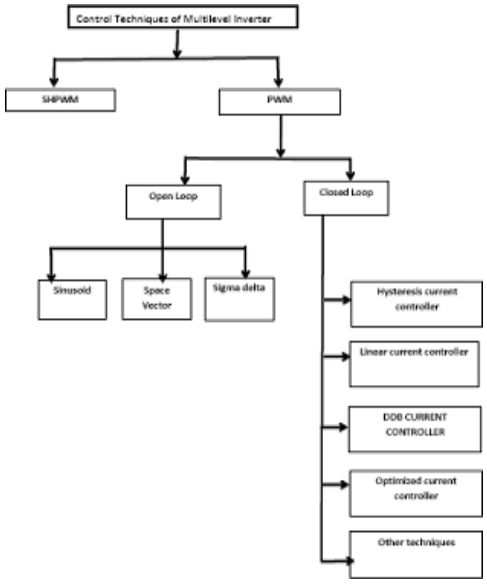

Fig.4 Control Techniques for a Cascaded H-Bridge MLI

Table.1 Switching sequence for 1–Φ7 level Cascade inverter

Output voltage	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
-3Vdc	0	1	1	0	0	1	1	0	0	1	1	0
-2Vdc	0	1	1	0	0	1	1	0	1	1	0	0
-Vdc	0	1	1	0	1	1	0	0	1	1	0	0
0Vdc	1	0	1	0	1	0	1	0	1	0	1	0
Vdc	1	0	0	1	0	0	1	1	0	0	1	1
2Vdc	1	0	0	1	0	0	1	1	1	0	0	1
3Vdc	1	0	0	1	1	0	0	1	1	0	0	1

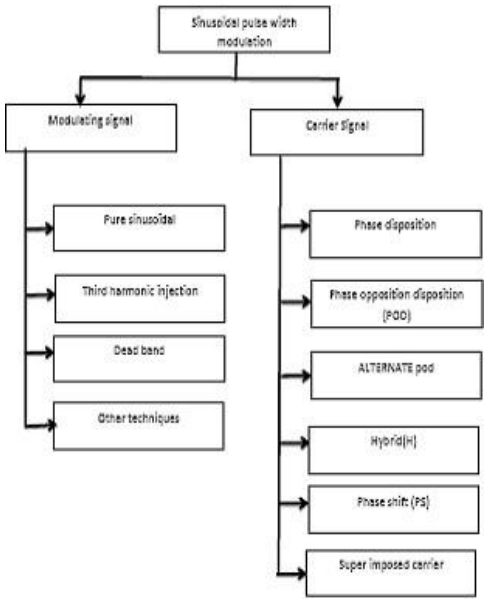

Fig.5 Classification of Sinusoidal PWM

In PWM technique also, sinusoidal PWM is used for generating triggering pulses to MLI. In sinusoidal PWM pure sinusoidal wave as modulating signal and multi carrier signal which is of triangular in shape have been considered. For an m-level MLI, (m-1) carrier signals are required. Multi carrier PWM techniques have sinusoidal signal as reference wave and triangular as carrier signals

Amplitude Modulation

Ma= Am/Ac(m−1) Frequency Modulation

Mf= Fc/Fr Ma = Amplitude of modulation wave Mf = Amplitude of carrier wave

Fc = Frequency of carrier wave

Fr = Frequency of Reference wave

In this topology we use the carrier wave modulation technique and sinusoidal modulation technique for the 7 level cascaded h bridge multi-level inverter and the THD value is

calculated and compared with the proposed topology The THD value of the 7 level cascaded H bridge inverter implemented with carrier wave modulation technique is 18,16%.

IV. TOPOLOGY [1]

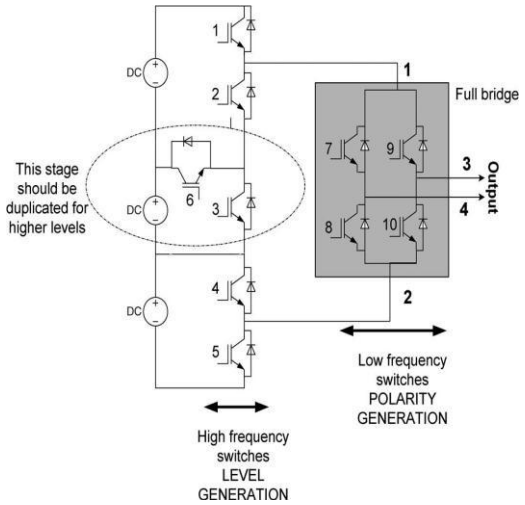

Fig.6 Configuration of Topology[1]

Here The topology[1] shown in the fig 6 is a hybrid multilevel topology which separates the output voltage into two parts. One part is named *level generation* part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability .The other part is called *polarity generation* part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency.

Table.2 List of DC input voltages to voltage levels

S.NO	LEVEL NUMBER	DC INPUT VOLTAGES
1	7	E,E,E
2	9	E,2E,E
3	11	E,2E,2E
4	13	E,3E,2E

The topology[1] uses isolated dc supplies. Therefore, it does not face voltage-balancing problems due to fixed dc voltage values Switching sequences in this converter are easier than its counter parts. According to its inherent advantages, it does not need to generate negative pulses for negative cycle control. Thus, there is no need for extra conditions for controlling the negative voltage. Instead, the reversing full-bridge converter performs this task, and the required level is produced by the high-switching- frequency component of the inverter. Then, this level is translated to negative or positive according to output voltage requirements.

One of the promising advantages of the topology[1] is that it requires less high- switching-frequency components. High- frequency switches and diodes are expensive and are more prone to be damaged than low-frequency switches.As the number of high-frequency switches is increased, the reliability of the converter is decreased. It can clearly be inferred that the number of components of the topology[1] is lower than that of other topologies even more so as the voltage levels increase and it will decrease tremendously with higher voltage levels.

V. PROPOSED TOPOLOGY

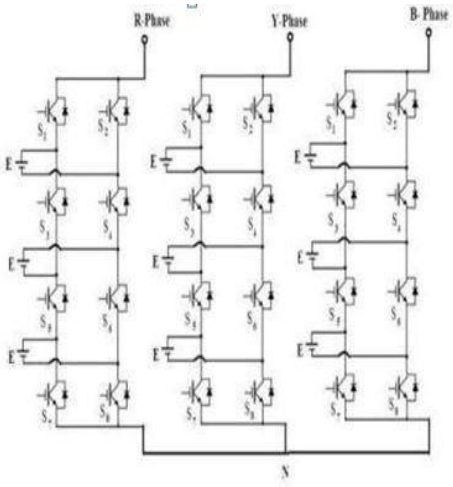

Fig 7: Three phase pattern of the proposed topology

The 7 level Inverter is designed with the less number of switches such that the complexity nature of the inverter reduces which in turn improves the output waveform of the system.

Table.3 Switvhing pattern of 7 level inverter

Level Voltages	Switching Pattern							
	S1	S2	S3	S4	S5	S6	S7	S8
+3E	1	0	0	1	1	0	0	1
+2E	1	0	0	1	1	0	1	0
+E	1	0	0	1	0	1	0	1
0	1	0	1	0	1	0	1	0
-E	0	1	1	0	1	0	1	0
-2E	0	1	1	0	0	1	0	1
-3E	0	1	1	0	0	1	1	0

To obtain number of levels at the output side the values of DC sources has to consider as per Table 2.The proposed topology can easy to develop as compared to the cascaded H-bridge multilevel inverters and THD also reduced as compared to the cascade inverters.

The switching pattern of the 7 level proposed topology is

as follows such that the level outputs of the inverter are obtained. The switching pattern for 7-level inverter is tabulated in the Table 2 indicates switch is in ON position, 0 indicates switch is in OFF position. From the below table the gate pulses are evaluated for each switch.

VI. SIMULATION RESULTS

The simulation results of the 7 level cascaded H bridge inverter by using the carrier wave pulse width modulation technique and the topology[1] along with the simulation results of the proposed topology are shown below.

Cascaded 7 level MLI:

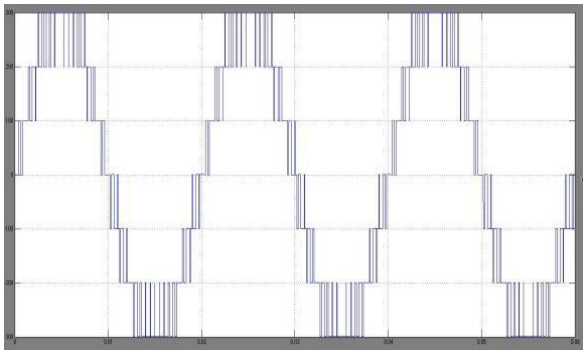

Fig8: Output voltage of the 7 level Cascaded MLI

(carrier pulse width modulation)

Topology[1]:

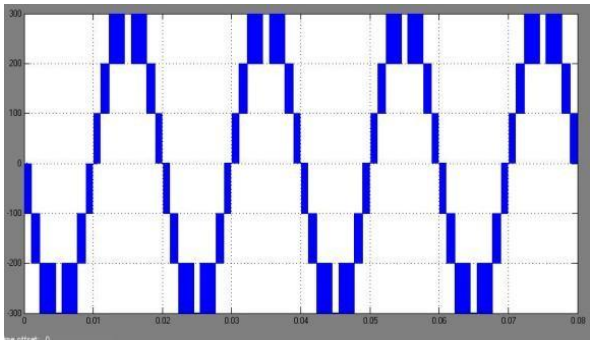

Fig7**:** Output Voltage of the 7 level Topology[1]

Proposed Topology:

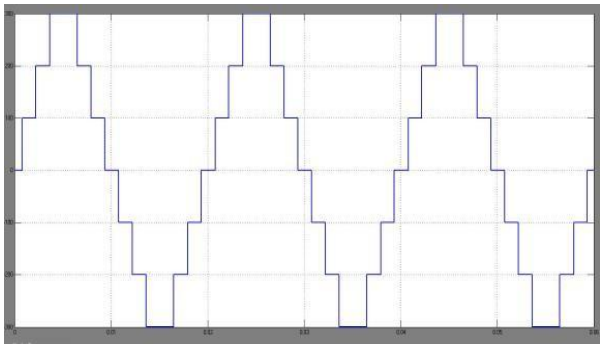

Fig 8**:** Output voltage of the proposed topology

The output voltages of the multi- level inverters are shown above. The FFT analysis of the cascaded MLI and the Asymmetrical MLI are also compared which gives the THD value of both the inverters.

FFT ANALYSIS

The FFT Analysis shows the level of reduction of the harmonic content in the inverters ie the harmonics are measured in the form of the Total Harmonic Distortion (THD).

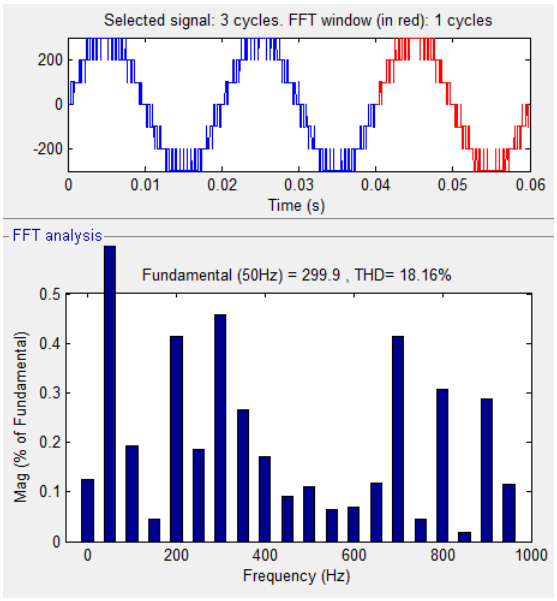

Fig 9: FFT Analysis of the 7 level new topology MLI

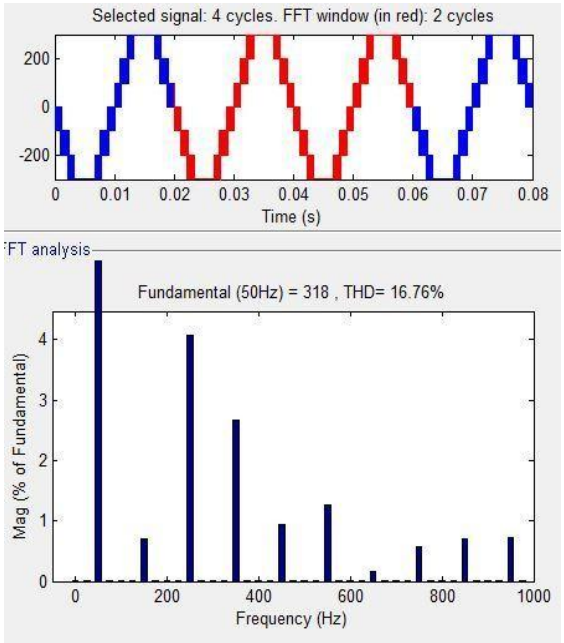

Fig10**:** FFT Analysis of the topology[1] (Carrier wave modulation)

Proposed Topology:

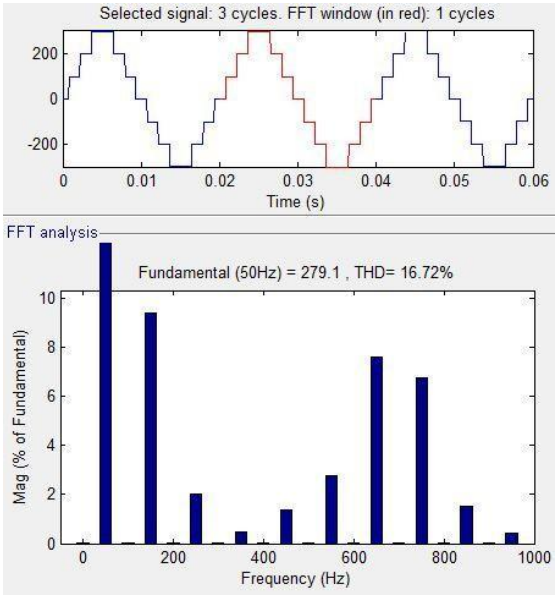

Fig11: FFT Analysis of the Proposed MLI

From the above FFT Analysis the THD value of the cascaded H bridge inverter is 18.16% which is reduced to 16.78% by using the topology[1] which gets reduced to 16.72% by using the proposed topology.

Table4: Comparision of MLI

Inverter type		Diode-clamp	Flying capacitor	CHBMLI	Topology[1]	Proposed Topology
Main switching devices	High frequency	(M-1)× 2	(M-1)× 2	(M-1)× 2	(M-1)	(M+1)
	Low frequency	0	0	0	4	0
Main diodes		(M-1)×2	(M-1)×2	(M-1)×2	(M-1)+4	(M+1)
Clamping Diodes		(M-1)× (M-2)	0	0	0	0
DC bus Capacitors		(M-1)	(M-1)	(M-1)/2	0	0
Balancing Capacitors		0	(M-1)× (M-2)/2	0	0	0

Table 5: THD COMPARISION

Inverter type	CHBMLI	Topology[1]	Proposed Topology
THD	18.23%	16.76%	16.72%

By which we can say that the value of THD gets reduced from 18.16% to 16.72% by using the proposed topology than the Cascaded multi level inverter

VII. CONCLUSION

The simulations of the seven-level Cascaded H bridge inverter , topology[1] and proposed topology[1] are successfully executed by using multi carrier pulse width modulation technique..The reduction of THD values are shown above from simulation results. This proposed topology can be further extended by using different modulation techniques such as SHE PWM, Space Vector Modulation etc.

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