Design and Analysis of 18 nm Graphene/TiO_2/$TiSi_x$ NMOS Device using Taguchi Method

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ABSTRACT

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been steady growth in high-speed switching applications in the semiconductor industry. The conventional combination of regular has to be replaced with high-k materials due to the limitation of shrinking the transistors. In this paper, Silicon Dioxide (SiO_2) and Polysilicon gate structure has been replaced with high-k materials and metal gate which are Titanium Dioxide (TiO_2) and Titanium Silicide ($TiSi_x$) respectively. The main objectives of this project are to reduce the leakage current (I_{OFF}) and optimum threshold voltage (V_{TH}) for the NMOS device. The designed and analyzed NMOS will be demonstrated in Silvaco software with ATHENA as a virtual fabrication process and ATLAS as analyzing the electric properties of the device. The results have been analyzed using Taguchi L9 orthogonal array method to obtain nominal values of threshold voltage and minimum value of leakage current. The initial results before optimizing with the Taguchi Method are 0.500061 V for V_{TH} and 13.2042 pA/µm for I_{OFF}. Once the device is optimized with Taguchi Method, the optimum value for V_{TH} is 0.540576 V and 12.9181 pA/µm for I_{OFF}. These values are met with the targeted values based on International Technology Roadmap for Semiconductors (ITRS) projection.

Keywords—NMOS, Taguchi, MOSFET, high-k

INTRODUCTION

In this study, an 18 nm NMOS device was designed through simulation as a virtual fabrication, featuring a gate structure composed of bilayer graphene, titanium dioxide (TiO_2) as the high-k gate dielectric, and titanium silicide ($TiSi_x$) as the metal gate. The primary objectives were to optimize the threshold voltage (V_{TH}), minimize leakage current, and facilitate continued transistor scaling in line with ITRS projections. The proposed device demonstrates strong potential for fabrication with desirable electrical characteristics, highlighting the effectiveness of the selected materials and device architecture. Nevertheless, the integration of high-k materials presents several challenges, including threshold voltage instability and susceptibility to short-channel effects (SCEs), all of which necessitate careful process optimization [1].

V_{TH} is the most fundamental parameter that determines whether the transistor can operate correctly in ON/OFF states. Significant deviation of V_{TH}, particularly due to short-channel effects, directly threatens device functionality and circuit stability. In close relation, I_{OFF} represents the leakage current when the device is in the OFF state, and its value is strongly influenced by V_{TH} stability. A lowered or unstable V_{TH} often leads to an increase in I_{OFF} due to weakened electrostatic gate control (e.g., drain-induced barrier lowering), making both parameters inherently coupled and critical for ensuring low-power operation and robust short-channel

suppression [2].

Moore's Law predicts that the number of transistors in dense Integrated Circuits (ICs) doubles approximately every two years [3]. While this trend has driven rapid advancements in semiconductor technology, silicon dioxide-based gate dielectrics are approaching fundamental physical limits, leading to increased leakage currents and short-channel effects as devices scale down [4]. Consequently, researchers have identified graphene/high-k/metal gate structures as promising alternatives for next-generation CMOS technology, capable of overcoming the limitations of conventional silicon gates [5] [6].

High-k materials are favored because the relatively high bandgap and low dielectric constant of polysilicon limit its effectiveness in controlling gate electrostatics, particularly in nanoscale devices [7]. Polysilicon exhibits a relatively high bandgap and a low dielectric constant [8]. The incorporation of a metal gate not only enables precise threshold voltage control and reduces gate resistance, but also allows for the elimination of certain unnecessary implants, thereby improving device reliability and performance at scaled nodes [9].

Graphene has been explored as a gate/interfacial material that can actively influence threshold voltage and off-state leakage by tuning its work function and by forming heterojunctions with silicon; such approaches have demonstrated improved V_{TH} control and reduced I_{OFF} in several recent experimental and theoretical studies [10][11].

In addition to material selection, process optimization plays a crucial role in achieving desirable device characteristics. Ion implantation, for instance, can be adjusted to control junction depths and lateral dopant distributions, which directly influence threshold voltage (V_{TH}), subthreshold leakage, and short-channel behavior . By carefully tuning the ion dose and implantation parameters, it is possible to mitigate short-channel effects, suppress off-state leakage (I_{OFF}), and enhance the overall performance of NMOS devices [12]. Together, the integration of high-k/metal gate stacks and systematic process optimization provides a viable pathway for fabricating highly scaled transistors for future technology nodes, which can be utilized in the design and production of next-generation transistors.

In this study, an 18 nm NMOS device was designed through simulation as a virtual fabrication, featuring a gate structure composed of bilayer graphene, titanium dioxide (TiO_2) as the high-k gate dielectric, and titanium silicide ($TiSi_x$) as the metal gate. The primary objectives were to optimize the threshold voltage (V_{TH}), minimize leakage current, and facilitate continued transistor scaling in line with ITRS projections. The proposed device demonstrates strong potential for fabrication with desirable electrical characteristics, highlighting the effectiveness of the selected materials and device architecture. Nevertheless, the integration of high-k materials presents several challenges, including threshold voltage instability, limited scaling potential, thermal reliability concerns, and susceptibility to short-channel effects (SCEs), all of which necessitate careful process optimization [1].

To address these challenges, the Taguchi method was employed in this study to systematically identify the critical process parameters influencing device performance. The Taguchi method enables optimization with fewer simulations while maintaining statistical robustness, thereby providing an efficient pathway to achieve the optimum electrical characteristics of the device [13].

METHODOLOGY

Fabrication Process (ATHENA)

Device construction was carried out using the ATHENA module, with High-k/Metal Gate (HKMG) technology applied during the fabrication process to realize the 18 nm metal gate. The design of the device involved specific adjustments tailored to the characteristics of the chosen materials and the device performance targets. Fig. 2 shows the fabrication process through the ATHENA simulation tools.

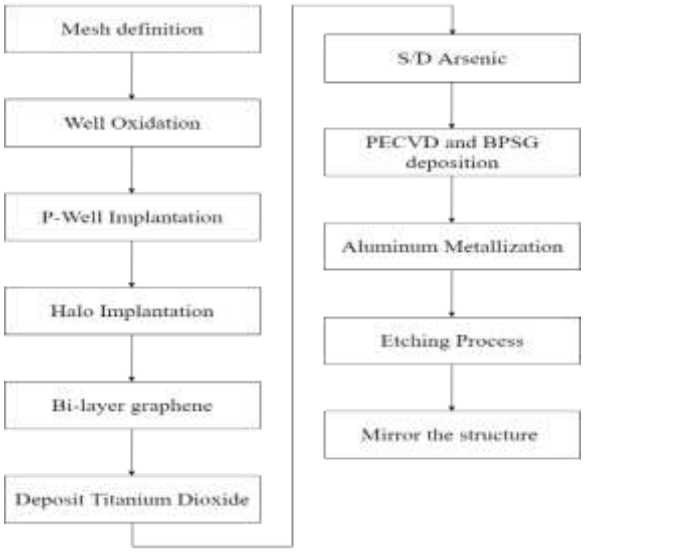

Fig. 1. 18 nm NMOS Fabrication in ATHENA

Device Simulation (ATLAS)

Once the virtual fabrication of the device was completed, the 18 nm NMOS was simulated in ATLAS to extract its characteristics and electrical properties. As shown in Fig. 3, the process was carried out using ATLAS simulation tools.

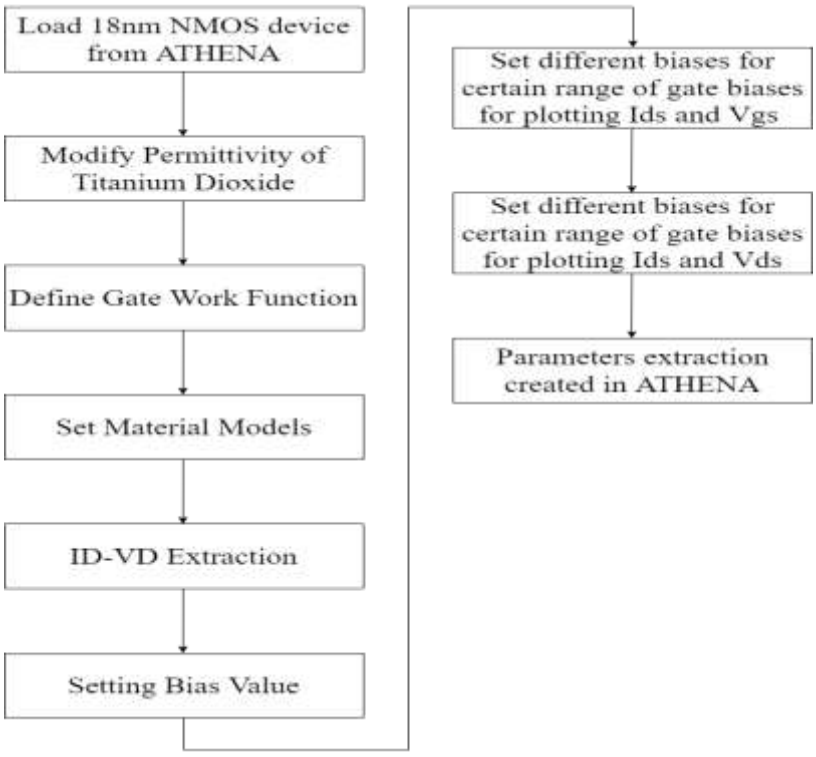

Fig. 2. Device simulation 18nm NMOS in ATLAS

Taguchi Orthogonal L9 Array

In Table 1, four process parameters are identified for optimization through the Taguchi method, which applies about 36 experimental simulations incorporating two noise factors. [14]. Hence, as shown in Table I, Factor A represents Halo Implantation, Factor B represents Halo Tilt Angle, Factor C represents S/D Implantation, and Factor D represents Compensation Implantation. In addition, two noise factors were considered in the experiments: Factor X, corresponding to the Sacrificial Oxide Layer (PSG), and Factor Y, corresponding to the

Oxide Temperature (BPSG), as listed in Table II.

Control Factors

Process Parameter	Unit	Level 1	Level 2	Level 3
Halo Implantation dose	atom/cm^3	2.852x10^3	2.857x10^3	2.862x10^3
Halo Implantation Tilt Angle	degree	33	35	37
S/D Implantation dose	atom/cm^3	4.77x10^3	4.8x10^3	4.83x10^3
Compensation Implantation	atom/cm^3	2.343x10^3	2.393x10^3	2.443x10^3

Noise Factors

Noise Factor	**Unit**	**Level 1**	**Level 2**
Sacrificial Oxide Layer (PSG)	°C	950	953
Oxide Temperature (BPSG)	°C	920	923

RESULTS AND DISCUSSION

Virtual Fabricated (ATHENA)

An 18 nm gate length is shown in the final structure of a planar NMOS device indicated as in Fig. 4.

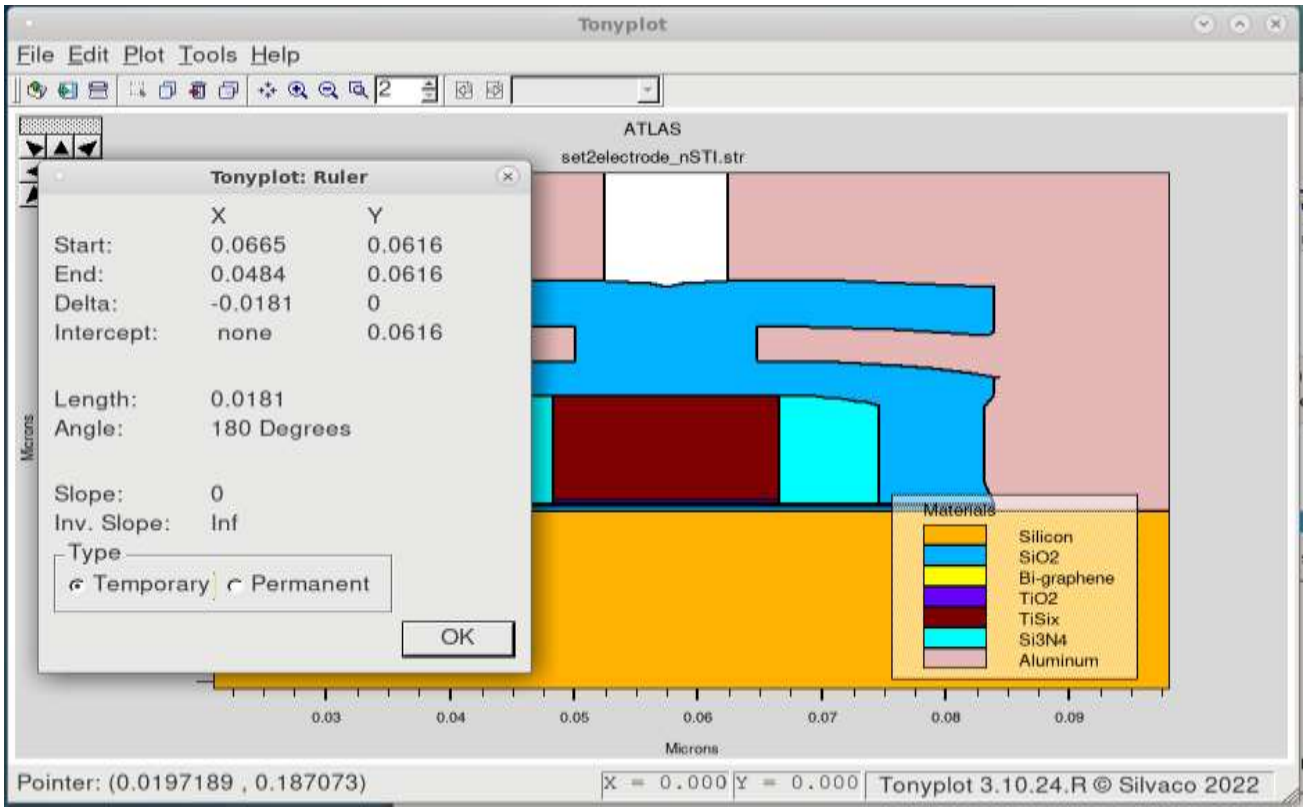

Fig. 3. 18nm NMOS device using Graphene/TiO_2/$TiSi_x$

Electrical Properties (ATLAS)

Fig. 5 and Fig. 6 show the electrical properties of the virtual fabricated 18 nm NMOS device designed in ATHENA.

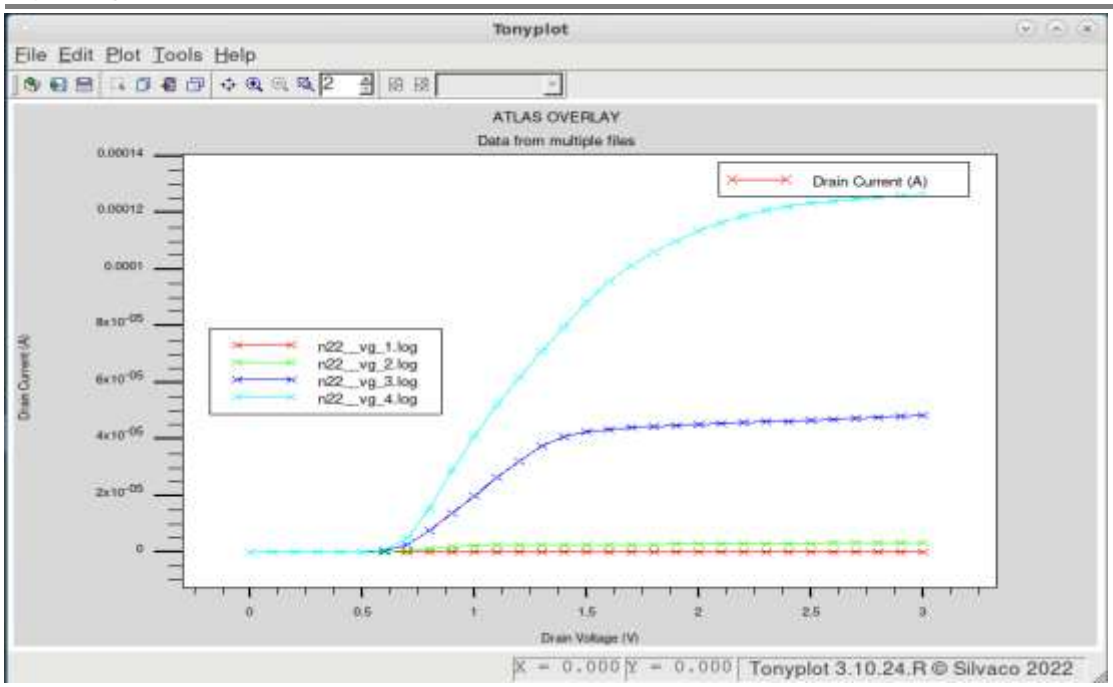

Fig. 4. I_D-V_{DS} characteristic of the 18nm NMOS device

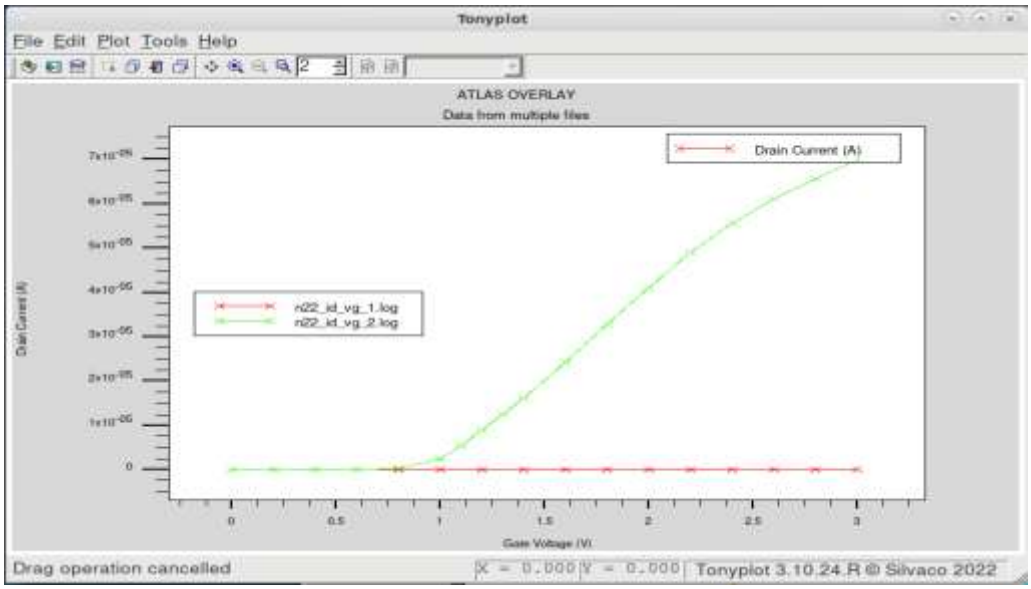

Fig. 5. I_D-V_{GS} characteristic of the 18nm NMOS device

Taguchi Method

The simulation results of the 36 experiments are shown in Table III and Table IV.

V_{TH} Results For Nmos Device

Expt. No.	Vth1 (X0,Y0)	Vth2 (X0,Y1)	Vth3 (X1,Y0)	Vth4 (X1,Y1)
1	0.679958	0.549870	0.548337	0.428199
2	0.490292	0.396658	0.413862	0.391097
3	0.389893	0.362519	0.383829	0.355165
4	0.652721	0.523257	0.524400	0.421650

5	0.461356	0.392629	0.409498	0.386703
6	0.402844	0.378700	0.397425	0.361534
7	0.620077	0.495027	0.495027	0.413796
8	0.545756	0.428467	0.432166	0.399982
9	0.398750	0.373752	0.393331	0.366571

I_{OFF} Results For Nmos Device

Expt. No.	**Ioff1 (X0,Y0)**	**Ioff 2 (X0,Y1)**	**Ioff 3 (X1,Y0)**	**Ioff 4 (X1,Y1)**
1	$12.8x10^{-12}$	$13.0x10^{-12}$	$25.6x10^{-12}$	$26.5x10^{-12}$
2	$13.2x10^{-12}$	$13.5x10^{-12}$	$27.5x10^{-12}$	$28.5x10^{-12}$
3	$13.7x10^{-12}$	$13.9x10^{-12}$	$29.9x10^{-12}$	$31.1x10^{-12}$
4	$12.8x10^{-12}$	$13.1x10^{-12}$	$25.9x10^{-12}$	$26.7x10^{-12}$
5	$13.3x10^{-12}$	$13.5x10^{-12}$	$27.9x10^{-12}$	$28.9x10^{-12}$
6	$13.5x10^{-12}$	$13.7x10^{-12}$	$28.8x10^{-12}$	$29.8x10^{-12}$
7	$12.9x10^{-12}$	$13.2x10^{-12}$	$13.2x10^{-12}$	$27.1x10^{-12}$
8	$13.1x10^{-12}$	$13.3x10^{-12}$	$26.9x10^{-12}$	$27.8x10^{-12}$
9	$13.6x10^{-12}$	$13.8x10^{-12}$	$29.2x10^{-12}$	$30.2x10^{-12}$

The Smaller-the-Better (STB) and Nominal-the-Best (NTB) performance characteristics were employed in the S/N ratio analysis [15]. The NTB characteristic was applied for the V_{TH} analysis, whereas the STB characteristic was used for the I_{OFF} analysis. Two tables are showing the S/N ratio for V_{TH} and I_{OFF}, respectively (see Table V and Table VI).

S/N RATIO FOR V_{TH}

S/N Ratio (Mean) (Nominal-the-Best)			Total mean
Level 1	Level 2	Level 3	S/N Ratio
20.30	20.96	20.11	20.45
15.01	19.30	27.05	
19.24	20.73	21.39	
21.4	20.33	19.63	

S/N RATIO FOR I_{OFF}

S/N Ratio (Mean) (Smaller-the-Better)			Total mean
Level 1	Level 2	Level 3	S/N Ratio
213.14	213.19	213.72	

214.16	213.20	212.68	213.35
213.31	213.19	213.55	
213.18	213.69	213.18	

ANOVA was applied to evaluate the contribution of each factor affecting device performance, with the results shown in Tables VII and VIII.

ANOVA ANALYSIS FOR V_{TH}

Process Parameter	Factor Effect (%)	
	NTB	Mean
Halo Implantation	0.51	0.16
Halo Tilt Angle	94.39	95.06
S/D Implantation	3.08	4.14
Compensation Implantation	2.02	0.64

ANOVA ANALYSIS FOR I_{OFF}

Process Parameter	Factor Effect (%)
	STB
Halo Implantation	13.06
Halo Tilt Angle	71.55
S/D Implantation	4.41
Compensation Implantation	10.98

In the factor analysis for V_{TH}, the Halo Tilt Angle was identified as the dominant factor, as it yielded the highest NTB factor effect. Conversely, S/D Implantation functioned more as an adjustment factor, showing a relatively low NTB value but a high Mean effect [16]. Hence, the S/D Implantation parameter was fine-tuned until the threshold voltage converged toward the nominal value projected by the ITRS. In the IOFF analysis, the Halo Tilt Angle again emerged as the dominant factor, contributing the highest factor effect of 10.98%. This dominance can be attributed to the Halo Tilt Angle's strong influence on short-channel effects and junction profile control, which directly impacts leakage current behavior in scaled NMOS devices, as also reported by previous researchers [17][18].

The S/D implantation dose was then varied, until closely aligned with the ITRS projection. Based on the experiments, the optimal dose was determined to be $4.65x10^{13}$. Table IX presents the best-projected process parameter settings obtained from the Taguchi method. The final parameters were simulated with noise factors to obtain the optimum results, and a confirmation experiment with additional noise factors is summarized in Table X. After optimization, the best threshold voltage of the 18 nm NMOS device was recorded at 0.540576 V, which falls within the ITRS specification which is 0.540 V ± 12.7% [19].

BEST SETTING SIMULATION FOR V_{TH}

Process Parameter	**Unit**	**Level**	**Best Value**
Halo Implantation dose	$Atom/cm^3$	2	$2.857x10^{13}$
Halo Implantation Tilt angle	degree	3	37

S/D Implantation dose	Atom/cm^3	Sweep	4.65x10^{13}
Compensation Implantation	Atom/cm^3	1	23.43x10^{13}

CONFIRMATION TEST RESULT FOR V_{TH}

V_{TH1}(X0,Y0)	**V_{TH2}(X0,Y1)**	**V_{TH1}(X1,Y0)**	**V_{TH1}(X1,Y1)**
0.540576	0.423995	0.428754	0.397208

For the leakage current (I_{OFF}) analysis, the optimal factor combination, corresponding to the highest STB values for each process parameter in Table VI was simulated, with the results summarized in Table XI. The lowest leakage current achieved was 12.9181 pA/μm, which is below the ITRS projected value, indicating an improvement in off-state device performance.

Finally, Table XIII presents the overall optimization results derived from the Taguchi method, together with a detailed comparison against the ITRS predictions to validate the effectiveness of the proposed process parameter tuning

BEST SETTING SIMULATION FOR I_{OFF}

Process Parameter	**Unit**	**Level**	**Best Value**
Halo Implantation dose	Atom/cm^3	3	2.862x10^{13}
Halo Implantation Tilt angle	degree	1	37
S/D Implantation dose	Atom/cm^3	3	4.83x10^{13}
Compensation Implantation	Atom/cm^3	2	23.93x10^{13}

CONFIRMATION TEST RESULT FOR I_{OFF}

I_{OFF1}(X0,Y0)	**I_{OFF2}(X0,Y1)**	**I_{OFF3}(X1,Y0)**	**I_{OFF4} (X1,Y1)**
12.9181x10^{-12}	13.1535x10^{-12}	26.1889x10^{-12}	27.0571x10^{-12}

COMPARISON V_{TH} AND I_{OFF} 18 NM NMOS DEVICE

Parameter	Value	ITRS projection
$V_{TH,}$ (V)	0.540576	0.540 ± 12.7%
I_{OFF} (pA/μm)	12.9181	<20

CONCLUSION

By first ensuring that V_{TH} and I_{OFF} are within an acceptable range, we establish the baseline stability of the device. If V_{TH} and I_{OFF} deviate too far from the target, further modeling or simulation may become irrelevant. Other analyses like example the mobility, gate capacitance, parasitics, temperature variation, process variation and interface behaviour will be addresses in future publications.

As a conclusions, an 18 nm NMOS device with a high-k/metal gate stack comprising bi-layer graphene, TiO_2, and $TiSi_x$ was successfully designed and optimized using Silvaco TCAD tools. The Taguchi L9 orthogonal array method was employed to systematically analyze the influence of process parameters on key electrical characteristics, namely threshold voltage (V_{TH}) and off-state leakage current (I_{OFF}). Factor analysis revealed that the Halo Tilt Angle was the dominant factor affecting both V_{TH} and I_{OFF}, while S/D Implantation acted as an

adjustment parameter to fine-tune the threshold voltage toward the nominal value predicted by ITRS.

After optimization, the device achieved a threshold voltage of V_{TH} = 0.540576 V and a leakage current of I_{OFF} = 12.9181 pA/μm, both of which satisfy the ITRS projection. These results demonstrate that the application of the Taguchi method provides an effective approach for identifying critical process parameters and enhancing device performance. Overall, the findings confirm the potential of high-k/metal gate integration with advanced process optimization techniques for supporting further transistor scaling in future CMOS technologies.

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REFERENCES

1. F. A. Anizam, L. N. Ismail, N. Sihab, and N. S. Mohd Sauki, “Performance of High-k Dielectric Material for Short Channel Length MOSFET Simulated using Silvaco TCAD Tools,” J Electr Electron Syst Res, vol. 19, no. OCT2021, pp. 143–148, 2021.
2. L. Shi et al., “Investigation on gate oxide reliability under gate bias screening for commercial SiC planar and trench MOSFETs,” Mater Sci Semicond Process, vol. 174, no. January, p. 108194, 2024.
3. R. K. Ratnesh et al., “Advancement and challenges in MOSFET scaling,” Mater Sci Semicond Process, vol. 134, no. January, p. 106002, 2021.
4. H. Iwai, “Future of Nano CMOS Technology,” in Symposium on Microelectronics Technology and Devices, 2013, pp. 1–10.
5. Prerna, “Future MOSFET devices using high-k (TiO2) dielectric,” Int J Res Appl Sci Eng Technol, vol. 1, pp. 23–28, 2013.
6. N. H. N. M. Nizam, A. M. A. Hamid, F. Salehuddin, K. E. Kaharudin, N. F. Z. Abidin, and A. S. M. Zain, “Optimization of 14 nm double gate Bi-GFET for lower leakage current,” Telkomnika (Telecommunication Comput Electron Control, vol. 21, no. 1, pp. 195–202, 2023.
7. [7] M. Lalruatfela, H. Chakrabarti, R. Maity, A. Baidya, S. Baishya, and N. P. Maity, “A Compact Drain Current Model for Graded Channel DMDG Structure with High-k Material,” Silicon, vol. 14, no. 17, pp. 11363–11370, 2022.
8. R. D. Clark, “Emerging applications for high K materials in VLSI technology,” Materials. 2014.
9. J. Robertson and R. M. Wallace, “High-K materials and metal gates for CMOS applications,” Mater Sci Eng R Reports, vol. 88, pp. 1–41, Feb. 2015.
10. W. Zhou, T. Ma, Y. Tian, Y. Jiang, and X. Yu, “Dielectric engineered graphene transistors for high-performance near-infrared photodetection,” iScience, vol. 27, no. 3, p. 109314, 2024.
11. B. Khosravi Rad, A. H. Mehrfar, Z. Sadeghi Neisiani, M. Khaje, and A. Eslami Majd, “Effect of fabrication process on contact resistance and channel in graphene field effect transistors,” Sci Rep, vol. 14, no. 1, pp. 1–9, 2024, doi: 10.1038/s41598-024-58360-9.
12. M. I. Current, “The role of ion implantation in CMOS scaling: A tutorial review,” in AIP Conference Proceedings, 2019. doi: 10.1063/1.5127674.
13. I. Yahaya, A. H. Afifah Maheran, F. Salehuddin, and K. E. Kaharudin, “Taguchi Method for p-MOS Threshold Voltage Optimization with a Gate Length of 22nm,” Int J Nanoelectron Mater, vol. 16, no. 1, pp. 1–9, 2023.
14. A. H. A. Maheran, M. Pritigavane, N. H. N. M. Nizam, F. Salehuddin, and N. Sabani, “Taguchi Method Statistical Analysis on Characterization and Optimization of 18-nm Double Gate MOSFETs,” Int J Nanoelectron Mater, vol. 17, no. 4, pp. 549–555, 2024.
15. P. J. Ross, “Taguchi Techniques for Quality Engineering: Loss Function, Orthogonal Experiments, Parameter and Tolerance Design,” Loss Fuction, Orthogonal Exp Param Toler Des, 1995.
16. A. H. Afifah Maheran, P. S. Menon, I. Ahmad, and S. Shaari, “Effect of Halo structure variations on the threshold voltage of a 22nm gate length NMOS transistor,” Mater Sci Semicond Process, vol. 17, pp.

155–161, Jan. 2014.
17. A. Erlebach, T. Feudel, A. Schenk, and C. Zechner, “Influence of HALO and drain-extension doping gradients on transistor performance,” Mater Sci Eng B, vol. 114–115, pp. 15–19, Dec. 2004.
18. A. H. Afifah Maheran et al., “Minimum leakage current optimization on 22 nm SOI NMOS device with HfO2/WSix/Graphene gate structure using Taguchi method.,” J Phys Conf Ser, vol. 1502, no. 1, 2020.
19. ITRS, “ITRS Report.” [Online]. Available: https://www.itrs2.org/itrs-reports.html