Investigation on Solar Power System via Field Programmable Gate Array

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ABSTRACT

In contemporary society, energy plays an essential role in daily life, powering applications such as lighting, heating, and other utilities in residential and educational settings. Over the past century, various energy sources have been utilized, including coal, oil, and natural gas. These energy sources are generally categorized into two types: non-renewable and renewable energy. Among the renewable options, solar energy has gained significant attention due to its capability to convert light energy into electrical energy. Consequently, solar-powered systems have been developed to harness sunlight and transform it into usable electrical power. However, the performance of solar panels is highly dependent on sunlight availability. During rainy or cloudy conditions, the energy output declines, often resulting in insufficient power to charge storage batteries. To address this issue, the proposed prototype is designed to ensure stable power delivery for safe and efficient battery charging. Furthermore, to maximize the utilization of solar energy, a buck-boost converter will be implemented to optimize system efficiency. This project aims to investigate a battery charging and discharging algorithm using FPGA technology and to evaluate the power delivery performance of the system.

Keywords: FPGA, Solar Power System, Buck-Boost Converter.

INTRODUCTION

A solar-powered system is a technology that converts solar energy into electrical energy [1]. It represents a renewable energy alternative that can replace conventional non-renewable sources [2]. Specifically, the system comprises a solar panel, which captures solar energy during daylight hours, and a battery, which stores the harvested energy for use during periods without sunlight, such as at night [3].

In a solar power system, the battery serves as a critical energy storage component. To ensure optimal performance and longevity, a battery charging system is employed to prevent overcharging and thereby extend the battery's lifespan [1], [3]. One common control approach in such systems is Pulse Width Modulation (PWM), which regulates the charging process based on the solar panel voltage by adjusting the duty cycle through a voltage controller [4]. However, the PWM method inherently maintains a fixed output voltage, which can limit the amount of extractable power [4]. Consequently, there is a need to investigate methods for improving power conversion efficiency.

In this study, a Field-Programmable Gate Array (FPGA) is utilized to process input signals from current sensors, monitor battery levels, assess solar power availability, and determine suitable charging and

discharging operations. This approach aims to ensure stable, efficient, and safe operation of the solar-powered system [5].

Prior to the introduction of Field-Programmable Gate Arrays (FPGAs), custom integrated circuits (ICs) were commonly employed to reduce system complexity, lower manufacturing costs, and enhance overall system performance [6], [7]. However, the design and development of custom ICs are both time-consuming and costly [4]. To address these limitations, FPGAs were introduced as versatile semiconductor devices that can be programmed to implement a wide range of algorithms [5]. Compared to custom ICs, a key advantage of FPGAs lies in their ability to be dynamically reconfigured [5]. This reconfiguration process can modify part or all of the FPGA's fabric resources, functioning similarly to loading a program into a processor [4].

The basic architecture of an FPGA comprises several fundamental elements, including lookup tables (LUTs), flip-flops (FFs), interconnecting wires, and input/output (I/O) pads. Each of these components performs distinct functions, collectively forming the core operational structure of an FPGA [5].

METHODOLOGY

MPPT Buck-Boost Converter

The Maximum Power Point Tracking (MPPT) buck–boost converter, as illustrated in Figure 1, shares similar circuit design characteristics with a conventional PWM-based buck–boost converter. However, in this design, the buck–boost configuration is implemented through the integration of two separate PWM signals, each dedicated to controlling the buck and boost functions independently.

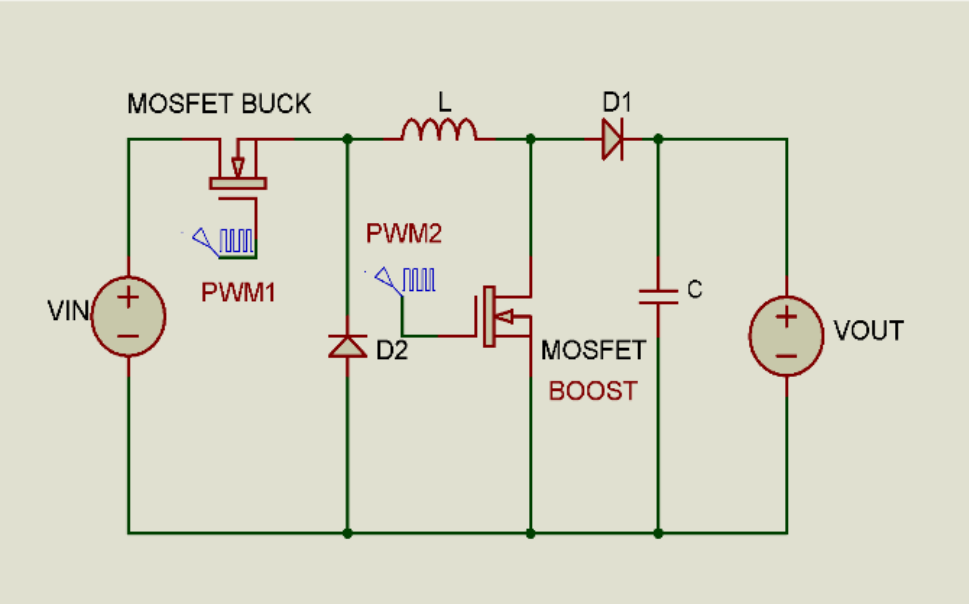

Figure 1. Buck-Boost Converter

In the buck–boost converter, the buck and boost operations are controlled through two independent signals, PWM1 and PWM2, each responsible for achieving the respective operating conditions. Table 1 presents the control states of PWM1 and PWM2 for implementing buck, boost, and combined buck–boost modes.

Table 1. PWM1 and PWM2 at different condition

Condition	***MOSFET BUCK***	***MOSFET BOOST***
Buck	Switching PWM1	PWM2=0
Boost	PWM1=1	Switching PWM2
Buck-boost	Switching PWM1	Switching PWM2

To determine the operating mode—buck, boost, or buck–boost—the voltage and current sensors measure the output parameters of the solar panel to calculate its power. Based on the implemented algorithm, the appropriate control signals for PWM1 and PWM2 are then generated to achieve the desired operating condition.

MPPT Algorithms

As illustrated in Figure 2, this project employs the Perturb and Observe (P&O) algorithm for Maximum Power Point Tracking (MPPT). In this method, the FPGA compares the solar panel power between two consecutive clock cycles. The algorithm considers three possible conditions: power remains constant, power decreases, or power increases. At the maximum power point (MPP), the measured power remains unchanged, and the DC–DC converter maintains its buck–boost operating state.

When the power changes, the corresponding voltage trend is also evaluated to determine the appropriate operating mode. If the power increases while the voltage decreases, the converter operates in buck mode; conversely, if the voltage increases, it operates in boost mode. Similarly, when the power decreases, a voltage decrease triggers buck mode, whereas a voltage increase results in boost mode. This control strategy ensures that the solar panel consistently operates at or near its maximum power point.

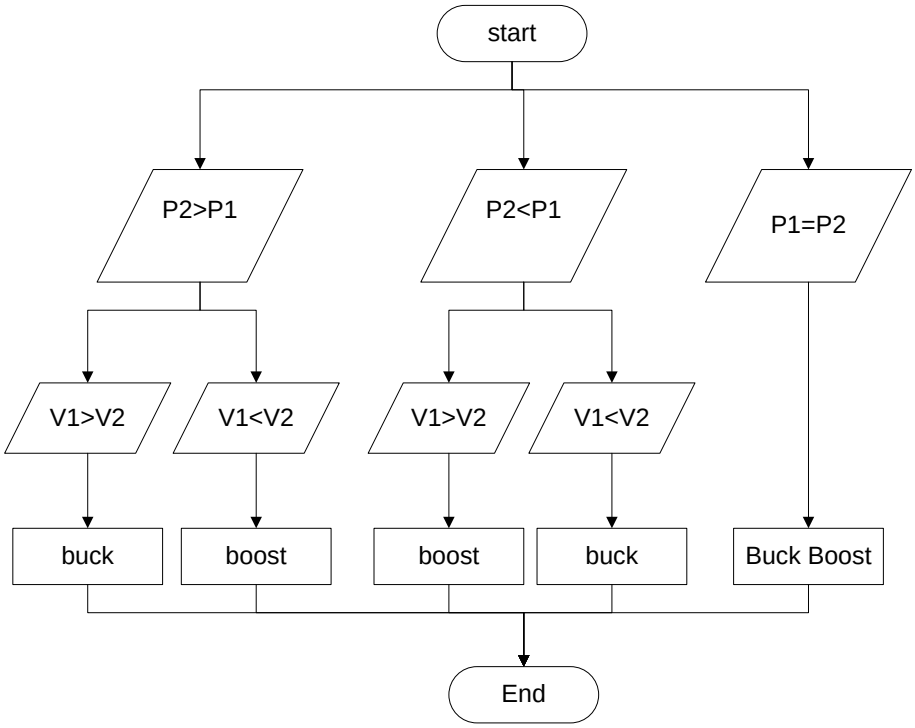

Figure 2. P&O Algorithm

Duty Cycle of the DC-DC converter

Since a buck–boost converter utilizes two PWM signals to control buck, boost, and buck–boost operations, the duty cycle of each PWM signal must be adjusted to extract the maximum power from the solar panel. As illustrated in Figure 3, the expected duty cycle patterns of PWM1 and PWM2 are used to regulate the converter's operating mode.

In the buck mode of the DC–DC converter, only the duty cycle of PWM1 is varied. Initially, the duty cycle is set to 0.4%, represented in Verilog code as a value of 1 out of 250. After each new cycle, this value is incremented by one until a change in operating condition is required. A similar approach is applied in the boost mode, except that PWM2 is used to switch and adjust the duty cycle. In the buck–boost mode, which corresponds to the maximum power point, the duty cycles of both PWM1 and PWM2 are fixed at 50%.

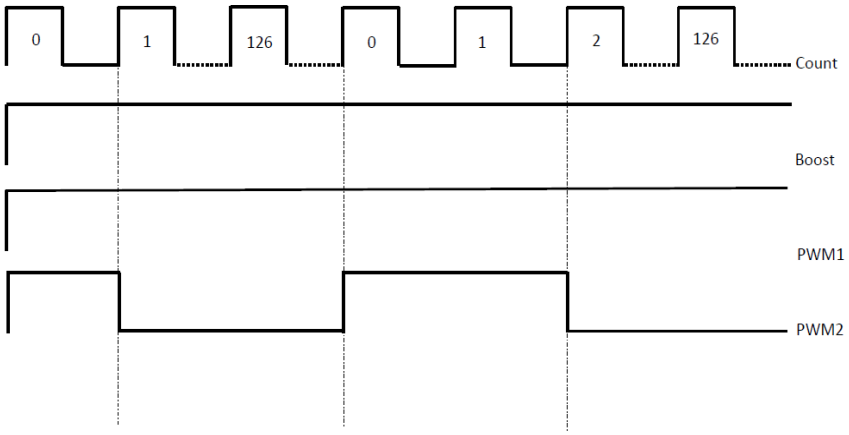

Figure 3. Boost Condition PWM1 and PWM2 signal

Lead Acid Battery Charging and Discharging Algorithm

The primary objective of developing this algorithm is to ensure that the battery is charged efficiently while preventing both overcharging and over-discharging. Once the maximum available power is extracted from the solar panel, the charging methodology must be carefully managed to prolong the battery's lifespan. As illustrated in Figure 4, charging and discharging flags are employed to indicate the operational stage of the algorithm.

When the algorithm enters charging mode, the charging switch is activated to monitor the battery voltage level. Upon reaching full charge—defined as 100% capacity or 12.7 V—the system terminates the charging process and transitions to discharging mode by setting the charging flag to '0' and the discharging flag to '1'.

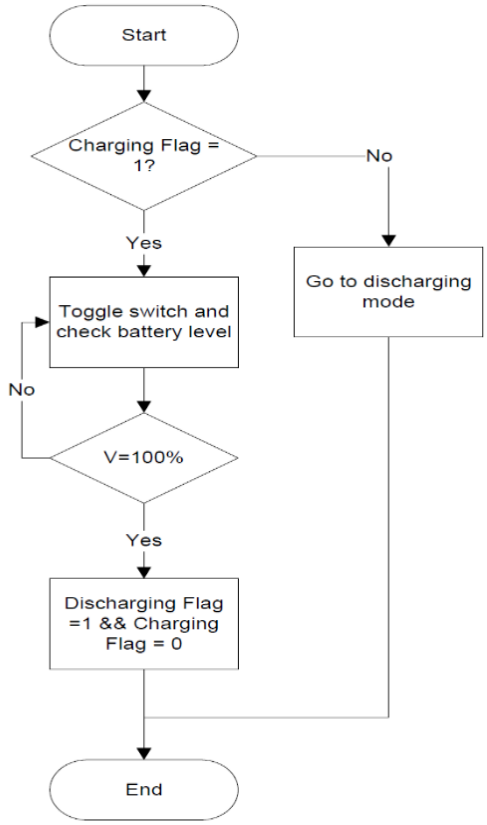

Figure 4. Charging Algorithm

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Upon completion of the charging process and attainment of full battery capacity, the discharging algorithm, as illustrated in Figure 5, is executed on the FPGA. The discharging algorithm operates similarly to the charging process, utilizing a discharging flag to manage operational states. When the battery voltage, as measured by the ADC converter, drops to 11V, the algorithm updates the discharging flag status from '1' to '0'.

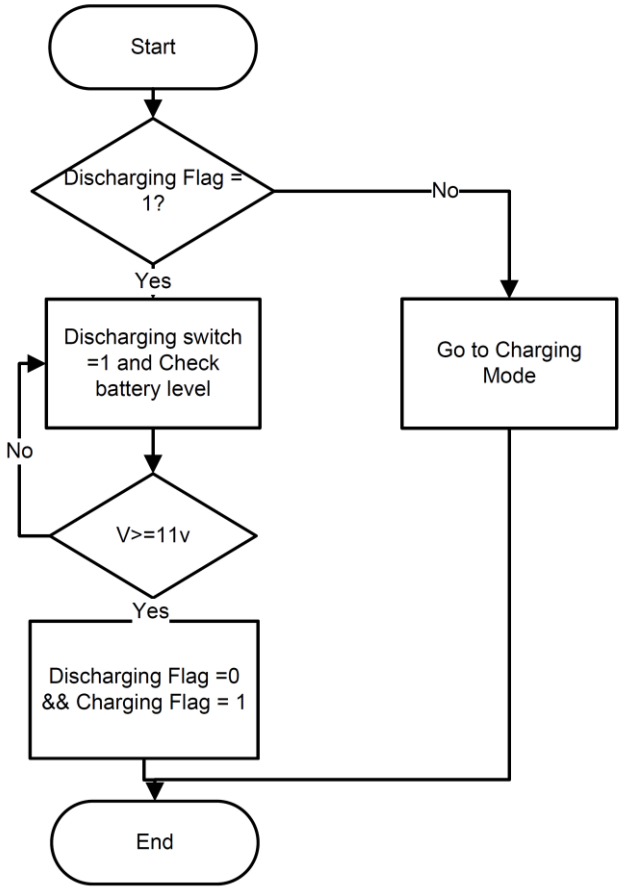

Figure 5. Discharging Algorithm

RESULTS AND DISCUSSION

The performance of the MPPT buck–boost converter will be evaluated through both simulation results and hardware implementation. The system comprises five main components: a frequency generator, power calculation module, comparator, and PWM signal generator. The comparator and PWM signal generator operate in three distinct modes—buck, boost, and buck–boost—depending on the control requirements.

Solar Power Calculation

In this section, the dedicated frequency generator clock counter, denoted as count2, is utilized to compute the values of power1 and power2 at different count intervals. Corresponding voltage measurements at these intervals are stored as vin1 and vin2. The purpose of storing these values is to enable comparison of voltage variations—whether an increase or decrease—after evaluating the power differences.

During simulation, the current value decreases with each clock cycle, while the voltage increases by one unit per cycle until reaching a binary value of 255, after which it resets to zero. This ensures that current and voltage values differ at every individual clock count. The results of the power calculation from the simulation are presented in Figure 6. Notably, the raw voltage input (vinraw) used for power computation is stored as vin1 and vin2, representing the voltage values at count2 equal to 100 and 200, respectively.

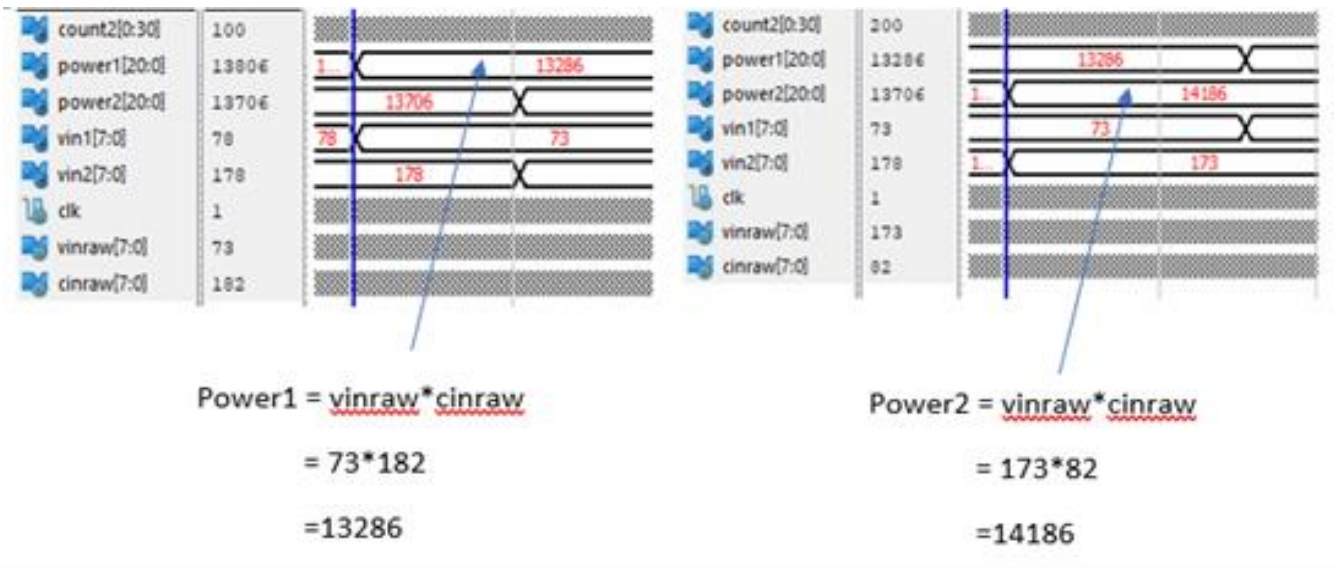

Figure 6. Power Calculation simulation result

MPPT Comparator

The MPPT comparator produces different output states—buck, boost, or buck–boost—based on the voltage and power values obtained from the power calculation sub-module. The selection process involves comparing the power between consecutive cycles, followed by evaluating the corresponding voltage changes.

As illustrated in Figure. 7, when the power decreases from 15,056 to 11,966 while the voltage increases from 93 to 193 in the subsequent clock cycle, the buck mode is selected. Conversely, when the power increases from 13,806 to 14,186 and the voltage rises from 73 to 173, the boost mode is selected.

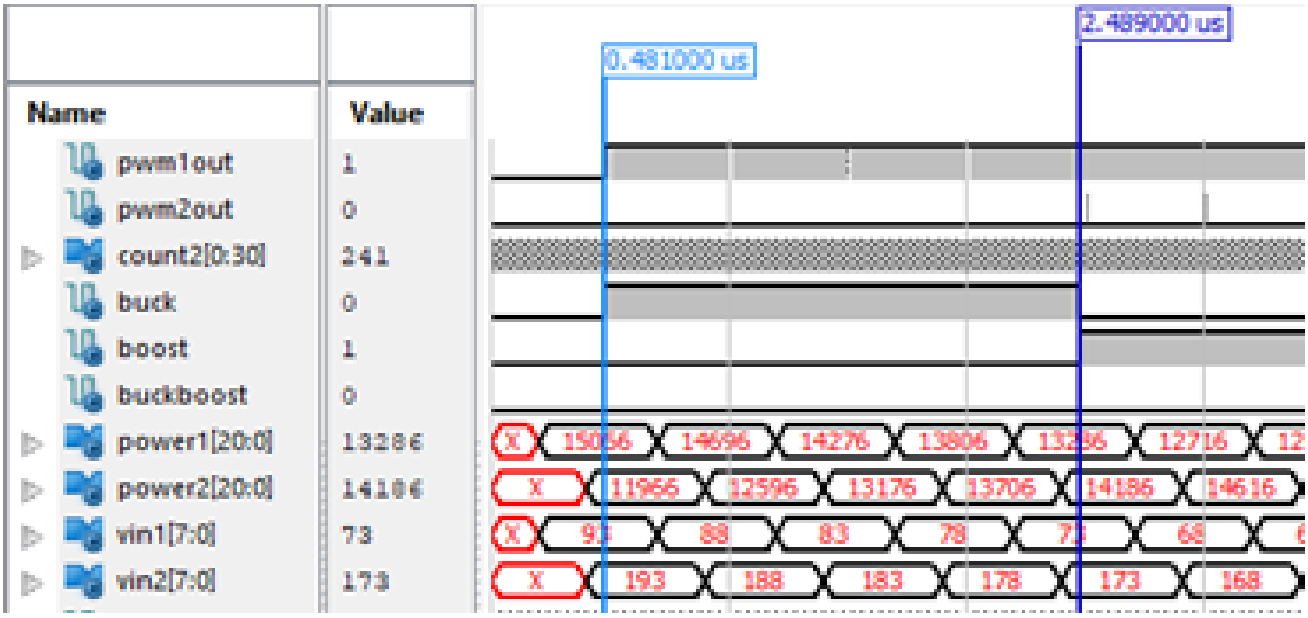

Figure 7. Comparator simulation result

Charging and Discharging Simulation

Upon completion of the MPPT simulation process, the charging and discharging algorithm for the solar system is executed. As shown in Figure 8, the discharging flag is activated when the battery level reaches a binary value of 251, triggering the closure (ON state) of switch2. This state is maintained until the battery level is detected at the threshold required to initiate the next charging cycle.

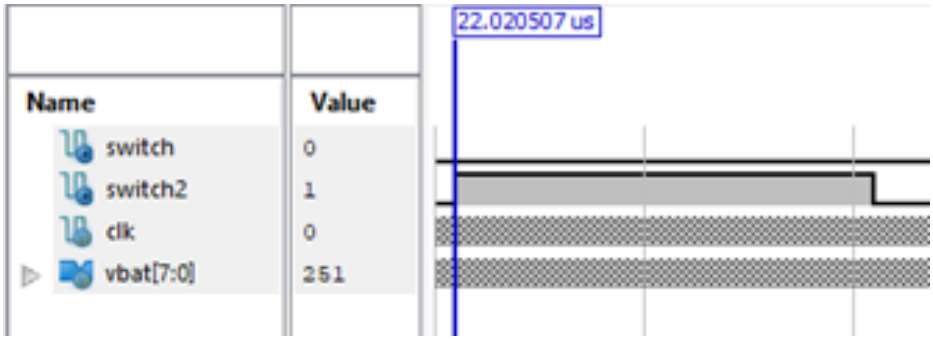

Figure 8. Discharging simulation result

During the charging stage, as illustrated in Figure. 9, the switch is opened (OFF state) for a total of 1005 clock counts to enable the charging process. This is followed by initiating the ADC conversion to measure the battery voltage. This approach ensures that the measurement reflects the actual battery level rather than the transient charging voltage.

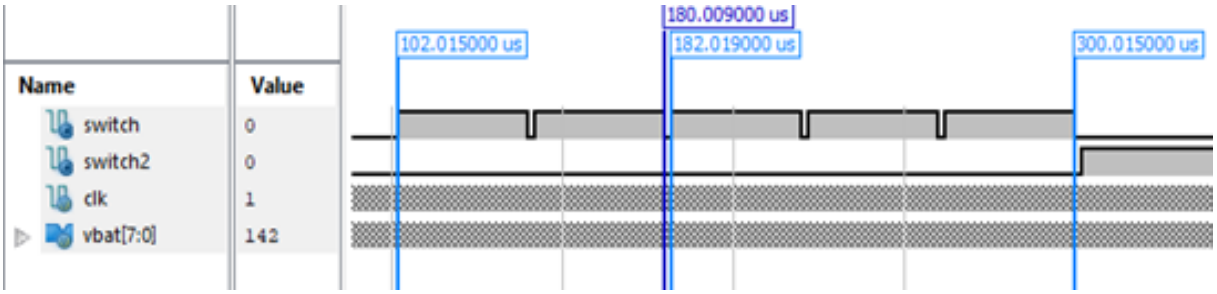

Figure 9. Charging simulation results

Analysis the efficiency of the Buck-Boost Converter

The DC–DC buck–boost converter prototype was implemented on a Xilinx Spartan-6 FPGA board, with on-board LEDs (LED0–LED2) indicating the operational status of buck, boost, and buck–boost modes. System performance and efficiency were evaluated by comparing the input power from the solar panel with the output power of the buck–boost converter. As shown in Figure 10, the prototype is driven by two MOSFET drivers to enable a fast-switching response to the FPGA-generated PWM signals.

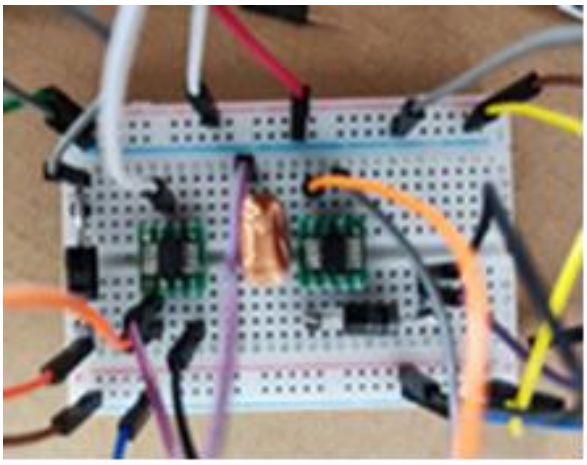

Figure 10. DC-DC Buck-Boost Converter

The performance data of the buck–boost converter was obtained using two multimeters: one measuring the output current and the other monitoring the output voltage, as illustrated in Figure 11. The recorded measurements from both the solar panel and the buck–boost converter is presented in Table 2.

Table 2. Reading of Solar Panel and DC-DC Converter

Solar panel input voltage (V)	Solar panel input current (A)	Power at Solar Panel (W)	Power at DC-DC converter (W)
14.94	0.105	1.5687	1.49
14.85	0.21	3.1185	2.95
15.30	0.843	12.8979	12.52
15.39	0.948	14.5613	13.82

$$efficiency = \frac{P_{out}}{P_{in}} \times 100\% \quad (1)$$

Based on the comparison, the proposed prototype achieved an efficiency of 95%, as calculated using equation (1).

CONCLUSION

In conclusion, the objectives of this project were successfully achieved. A prototype solar power system incorporating a DC–DC buck–boost converter was developed using a Xilinx Spartan-6 FPGA board. The proposed MPPT buck–boost converter achieved an efficiency of approximately 95%. Due to the low-voltage operating characteristics of the Xilinx Spartan-6 FPGA development board, specific low-voltage components were required, such as the 3.3 V AD7822 ADC and MOSFET drivers.

Several recommendations are proposed to further enhance the design of the FPGA-based solar power system. First, the buck–boost converter could be upgraded with a more advanced and efficient circuit topology, enabling compatibility with higher-power solar panels. For future work, it is suggested to investigate Maximum Power Point Tracking (MPPT) using fuzzy logic in conjunction with temperature and luminance sensors. A fuzzy logic–based control approach can adaptively determine the optimal duty cycle by processing a broader range of input data, thereby improving the efficiency of the DC–DC converter.

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