

Comparative Analysis of Latency, Throughput and Network Power for West First, North Last and West First North Last Routing Algorithm For 2D 4 X 4 Mesh Topology NoC Architecture

Bhupendra Kumar Soni¹, Dr. Girish Parmar²

¹Department of Electronics and Communication, Mewar University Chittorgarh, India

²Department of Electronics Engineering, Rajasthan Technical University Kota, India

Abstract — Network on Chip (NoC) is one of the proficient on-chip communication structural design for System on Chip (SoC) where a large number of computational and storage blocks are included on a single chip. NoC is one of today's emerging technology which has extend very fast to meet today's require of quick communication. Routing algorithm is an essential concept of Network on Chip. In this paper, we have used West-First, North Last and West First North Last routing algorithm in 2D Mesh 4 X 4 Topology of NoC Architecture using NIRGAM Simulator with Butterfly Traffic. The simulation results reveals the dominance of West-First, North Last and West First North Last routing algorithm depicting the minimum values of overall average latency per channel (in clock cycles per flit) as 1.22388 for WF overall average latency per channel (in clock cycles per packet) as 11.7143 for WF, average throughput as 85.005Gbps for WFNL, and total network power as 0.0221687mw, achieved for WFNL routing algorithm.

Index Terms - Butterfly traffic, Mesh Topology, Network-on-Chip, , North Last Routing Algorithm, West-First Routing Algorithm.

I. INTRODUCTION

Network on Chip (NoC) is a new prototype for System on Chip (SoC) blueprint. In NoC paradigm, cores are connected to each other through a network of routers and they communicate along with themselves throughout packet-switched communication. . It allows major reuse of resources and provides extremely scalable and elastic communication infrastructure for SoC design. Data interactions between segments of chip are packetized and transferred through the network. The network consists of wires, routers, processors, memories and other IP-blocks (Intellectual property) are connected to routers. A routing algorithm plays a important role on network's function. NOC permits a more consumption of communication resource than conventional on chip buses.

II. NETWORK TOPOLOGY

Topology is not anything but collection of nodes and channels within the network. A well-organized topology should be preferred for a network so that the performance will be get better and it can complete the bandwidth and latency requirement with low cost. Topology can be regular or irregular. A topology can be called non-blocking if it can manage and serve all the requirements coming to it. So the researchers proposed various topologies like Mesh, Torus, Tree, Butterfly, Star, and Spin. Different flow control mechanism is also called as switching techniques. Main task of switching technique is to set up connection between input and output channel inside the router. There are two types of well-liked switching techniques Circuit Switching Technique and Packet Switching Technique.

III. ROUTING ALGORITHM

A routing algorithm determines the whole path for the message or data packets to arrive at the destination. major task of a routing algorithm is to allocate the traffic from diverse nodes evenly all over the network. There are a few properties of routing algorithms which are basically necessary for interconnection networks i.e. connectivity, adaptivity, dead lock and live lock freedom. A particular routing algorithm affects the router propose complexity, area and hence affects the power consumption in whole network to get all performance necessities.

West First Routing Algorithm:

According to this algorithm a message must primary pass through in the West path (if necessary) before roaming in any other way. After travelling to WEST direction it can adaptively route through SOUTH, EAST and NORTH direction. Message can't be in retreat in WEST direction later on because of the routing boundaries applied. WF routing provides all possible shortest paths for the communication.

North Last Routing Algorithm:

According to this algorithm the message will be running scared in NORTH direction only if it is the last direction to be travelled. Once a message has turned North, no further turns are permitted; hence, the North turn must be made last. In this algorithm message is routed first adaptively in WEST, SOUTH and EAST direction and at last in NORTH direction. It is a partly adaptive routing algorithm. In mesh network it applies two routing restriction at any node i.e. North to West Turn and North to East Turn. The packets can't take a turn from NORTH port to WEST port or NORTH port to EAST port of a node.

West First North Last Routing Algorithm:

It provides all likely shortest paths for the communication. We use N, E, W, S to represent the North, East, West and South direction. For a 2-D Mesh topology, we can use (x, y) coordinates to identify each node. The Source and Destination addresses are represented as (Sxo, Syo), (Dxo, Dyo) respectively and current address as (Cxo, Cyo). Here $E_x = D_x - C_x$ and $E_y = D_y - C_y$

- When the source address and destination address are equal, then the packets are sent to local node.
- When the source address and destination address are not equal, the value of E_x and E_y must be compared i.e. when $E_x < 0$, E_y is not equal to zero, the packets are sent to West channel; When $E_x > 0$ and $E_y \geq 0$, the packets are sent to south channel; When $E_x = 0$ and $E_y > 0$ the packets are sent to North channel; When $E_x < 0$ and $E_y = 0$ the packets are sent to North channel.

IV. EXPERIMENTAL SETUP IN NIRGAM SIMULATOR

The experimental setups for the evaluation of the routing algorithms are 4x4 mesh topology where each node is connected with CBR (Constant Bit Rate) traffic generator. Buffer depth (number of buffers) of input channel FIFO is 32. The Warm up time is 1000, Sim_Num is 5000 and Tg-Num is 3000. Number of virtual channels per physical channel is 4. Link length is 3 μ m. Packet size is taken as 20 bytes with flit interval 2 clock cycles, clock frequency 1 GHz and Butterfly Mapping.

V. EXPERIMENTAL RESULTS

Performance analysis of West-First, North Last and West First North Last routing algorithm on various load 25%, 50%, 75% and 100% have carried out to compare Overall Average Latency per channel (in clock cycles per flit), Overall Average Latency per channel (in clock cycles per Packet), Total Network Power (in Mili Watt) and Throughput (in Gbps). The results we found are as follows.

Table1: Comparison of overall average latency per channel (in clock cycles per flit) for WF, NL, WFNL routing algorithms by Load variation

Overall Average Latency per channel (in clock cycles per flit)			
% of Load	WF	NL	WFNL
25	0.769231	1.03125	1.95455
50	1.15833	6.69801	2.0539
75	1.15833	6.69801	2.0539
100	1.22388	1.99324	10.6133

The following figure gives the simulation result of WF routing algorithm of 4x4 network size. The simulation result of Fig.1. Represents total network Power, Fig.2 represents Throughput, Fig. 3. Represents latency/flit, while Fig.4. Represents latency / packet.

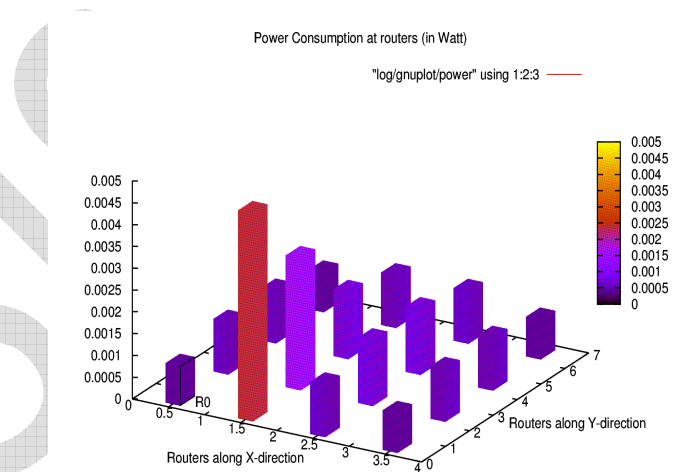


Fig.1: Power Consumption Graph for WEST FIRST Routing Algorithm

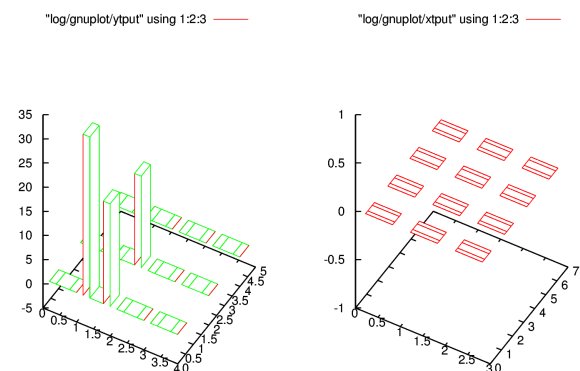


Fig. 2: Throughput Graph for WEST FIRST Routing Algorithm

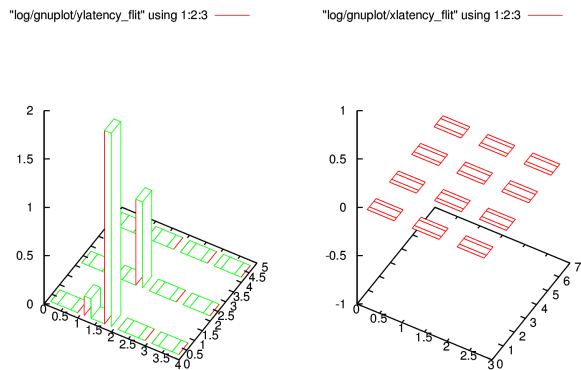


Fig. 3: Latency per Flit Graph for WEST FIRST Routing Algorithm

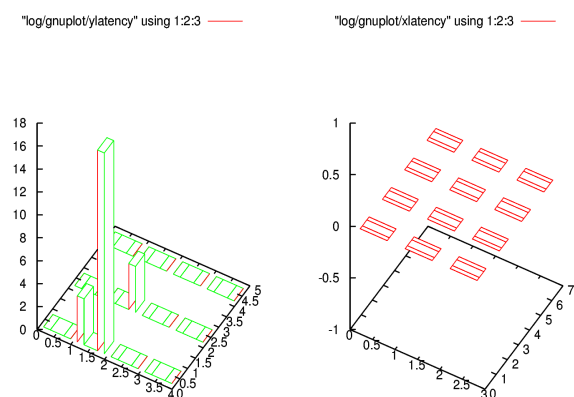


Fig. 4: Latency per Packet Graph for WEAST FIRST Routing Algorithm

The graphical representation of Table1. is shown below

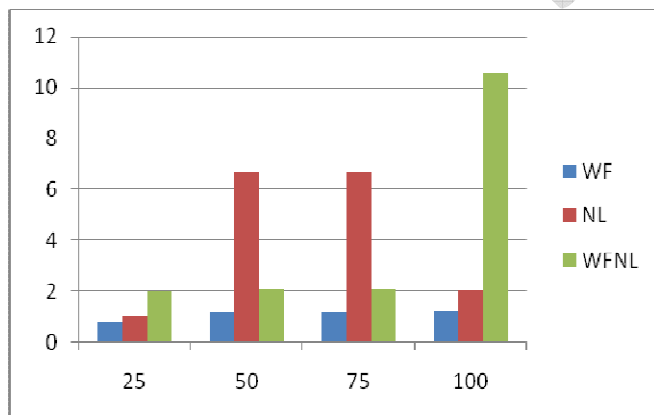


Fig.5: Graphical Representation of overall average latency per channel (in clock cycles per flit) for WF, NL, WFNL routing algorithms by Load variation

From the above figure it is clear that for WF Algorithm overall average latency per channel (in clock cycles per flit) is 1.22388.

Table2: Comparison of Overall Average Latency per channel (in clock cycles per Packet) for WF, NL, WFNL routing algorithms by Load variation

Overall Average Latency per channel (in clock cycles per Packet)			
% of Load	WF	NL	WFNL
25	7.77778	100.333	12.4222
50	9.92857	41.0897	12.7011
75	9.92857	41.0897	12.7011
100	11.7143	17.3529	65.5667

The table 2 shows Overall Average Latency per channel (in clock cycles per Packet) is 11.7143 for WF Routing Algorithm.

Fig.6 shows the graphical representation of Table-2

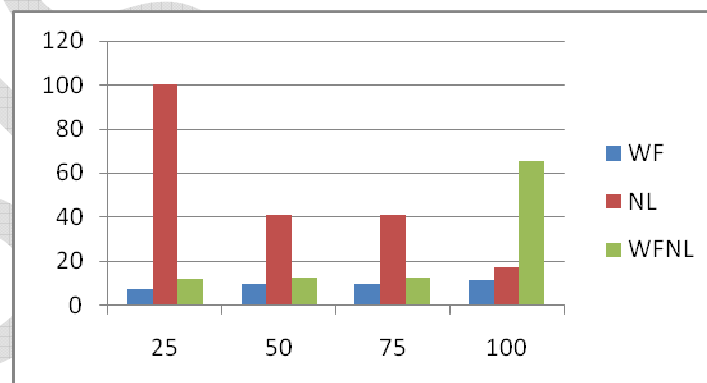


Fig.6: Graphical Representation of Overall Average Latency per channel (in clock cycles per Packet) for WF, NL, WFNL routing algorithms by Load variation

The table 3 below shows the comparison Total Network Power (in Mili Watt) for WL, NL, WFNL routing algorithms.

Table3: Comparison of Total Network Power (in Mili Watt) for WF, NL, WFNL routing algorithms by Load variation

Total Network Power(in Mili Watt)			
% of Load	WF	NL	WFNL
25	0.023465	0.0249332	0.0204175
50	0.0249906	0.0316253	0.0220144
75	0.0249906	0.0316253	0.0220144
100	0.0240942	0.0270275	0.0221687

Fig.7 shows the graphical representation of Table-3

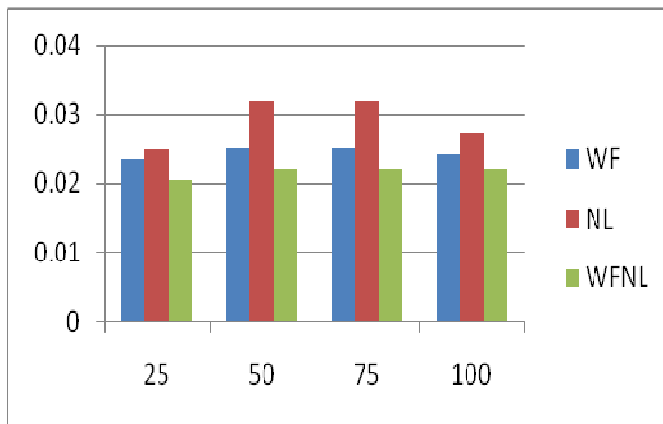


Fig.7: Graphical Representation of Total Network Power (in Mili Watt) for WF, NL, WFNL routing algorithms by Load variation

The table 4 below shows the comparison Throughput (in Gbps) for WL, NL, WFNL routing algorithms.

Table4: Comparison of Throughput (in Gbps) for WF, NL, WFNL routing algorithms by Load variation

Throughput (in Gbps)			
% of Load	WF	NL	WFNL
25	47.58	73.605	84.98
50	67.72	66.43	85.005
75	67.72	66.43	85.005
100	73.37	86.43	84.98

Fig.8 shows the graphical representation of Table-4

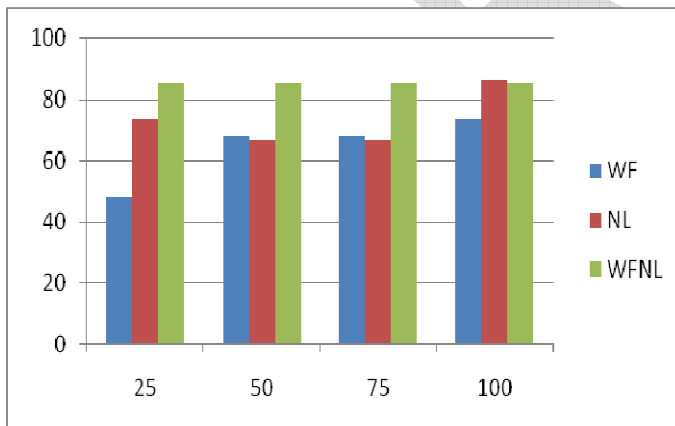


Fig.8: Graphical Representation of Throughput (in Gbps) for WF, NL, WFNL routing algorithms by Load variation

The following figure gives the simulation result of NL routing algorithm of 4x4 network size. The simulation result of Fig.9. Represents total network Power, Fig.10 represents Throughput, Fig. 11. Represents latency/flit, while Fig.12. Represents latency/packet.

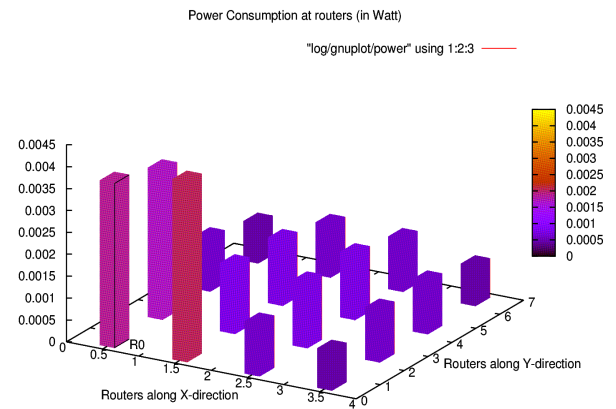


Fig.9: Power Consumption Graph for NORTH LAST Routing Algorithm

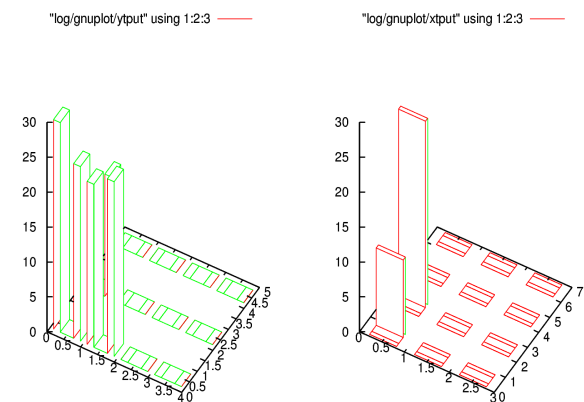


Fig. 10: Throughput Graph for NORTH LAST Routing Algorithm

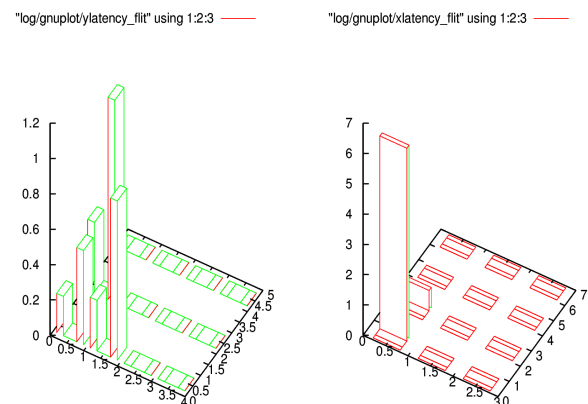


Fig.11: Latency per Flit Graph for NORTH LAST Routing Algorithm

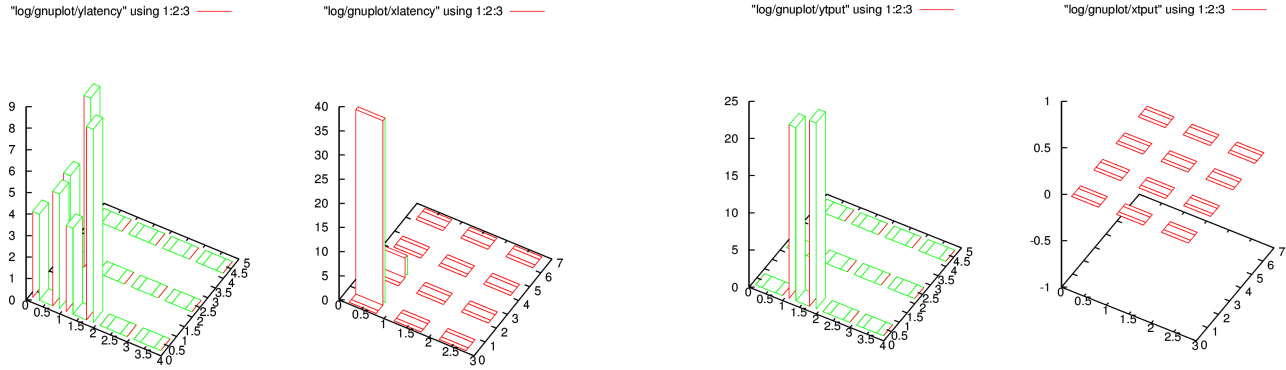


Figure12. Latency per Packet Graph for NORTH LAST Routing Algorithm

The following figure gives the simulation result of FWNL routing algorithm of 4x4 network size. The simulation result of Fig.13. Represents total network Power, Fig.14 represents Throughput, Fig. 15. Represents latency/flit, while Fig.16. Represents latency/packet.

Figure15 . Latency per Flit Graph for FIRST WEST NORTH LAST Routing Algorithm

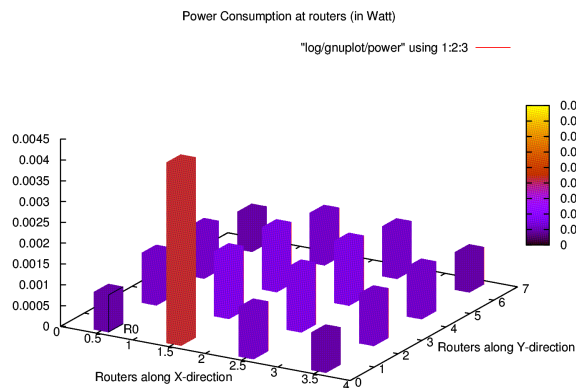


Fig.13: Power Consumption Graph for FIRST WEST NORTH LAST Routing Algorithm

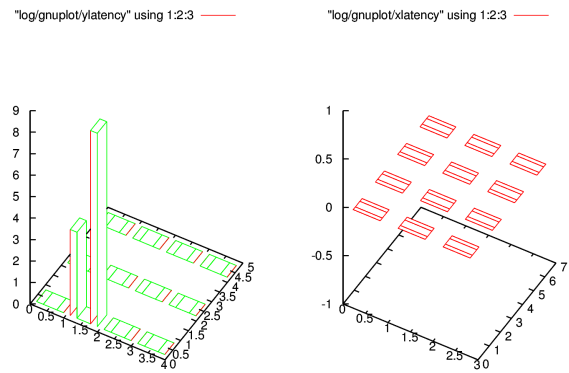


Fig.16: Latency per Packet Graph for FIRST WEST NORTH LAST Routing Algorithm

Performance metrics is the ratio between average throughput and average latency. More the “P” better the Routing Algorithm.

P = Performance Metrics (Per channel basis)

$$P = \frac{\text{Average Throughput}}{\text{Average Latency}}$$

For WF Routing (100% Load) $P = (4.817/11.7143) = 0.41120$

For NL Routing (100% Load) $P = (11.5241/17.3529) = 0.39623$

For WFNL Routing (100% Load) $P = (5.6656/65.5667) = 0.08640$

VI. CONCLUSION

The paper represents the performance Analysis of Latency, Throughput and Network Power for West First, North Last and West First North Last Routing Algorithm For 2D 4 X 4

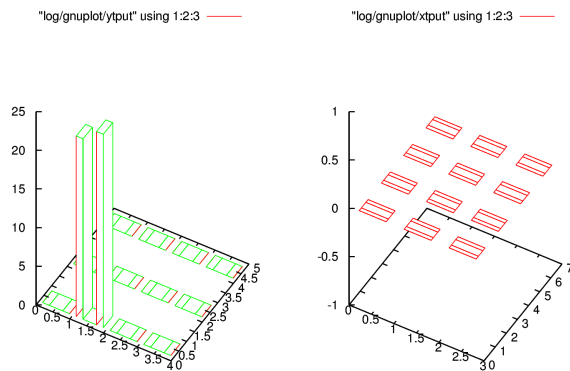


Fig.14 : Throughput Graph for FIRST WEST NORTH LAST Routing Algorithm

Mesh Topology NoC Architecture with variation of Load 25%,50%,75%,100% using butterfly mapping.

It has been observed that West First North Last Routing Algorithm is finest. The comparison results in Table 3 and Table 4 show that in context total network Power and Throughput West-First proves to be most excellent compared to WF and NL Routing Algorithm.

REFERENCES

- [1]. Vaishali V.Ingle, Mahendra A. Gaikwad, *Mesh Topology of NoC Architecture Using Source Routing Algorithm*" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-2, Issue-6, August 2013
- [2]. T. Bjerregaard and S. Mahadevan, *A Survey of Research and Practices of Network-on-Chip*" ACM Computing Surveys, Vol. 38, March 2006, Article 1.
- [3]. N.Ashokkumar, P. Nagarajan, S.Ravanaraja, *Survey Exploration of Network-on-Chip Architecture*"
- [4]. U. Y. Ogras and R. Marculescu, *Modeling, Analysis and Optimization of Network-on-Chip Communication Architectures*, Lecture Notes in Electrical Engineering 184, DOI: 10.1007/978-94-007-3958-1_2, _ Springer Science+Business Media New York 2013
- [5]. Ankur Agarwal, Cyril Iskander, Ravi Shankar, *Survey of Network on Chip (NoC) Architectures & Contributions*"Journal of Engineering,Computing and Architecture ISSN 1934-7197
- [6]. Monika Gupta, S. R. Biradar, B. P. Singh, *OPEN SOURCE SIMULATOR FOR NETWORK ON CHIP*" International Journal of Computers & Technology Volume 4 No. 2, March-April, 2013, ISSN 2277-3061

RSIS