Comparison of High Speed & Low Power Techniques GDI & McCMOS in Full Adder Design

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Abstract- **In modern era, VLSI technology has focussed for enhancing the performance, less power requirement and high speed of any digital circuit. Due to scaling style, power dissipation, propagation delay and transistor count (area) need to be concern by VLSI designer as per the application. Any digital circuit whose performance affect the entire system performance need to be focused more for power consumption and delay. Full adder is such circuit of great interest and whose modification would directly or indirectly effect the performance of entire system. Thus, reducing the power dissipation of full adder will ultimately reduce the power dissipation of the system. It is used for many application such as digital signal processing, microprocessor, and in data processing unit. Now-a-days, numerous efficient techniques are used for designing a VLSI circuit. This paper describes the design and analysis of full adder using two technique GDI (Gate Diffusion Input) and McCMOS (Multi-Channel CMOS) and comparing on the bases of different constraints such as power, propagation delay, pdp (power delay product), area and the performance of two. Even though both are low power and high speed techniques but it is observed that McCMOS style of designing have 8.09% less power dissipation and approx. 10.5% reduced power delay product as compared to GDI in a full adder design. But it is also observed that number of transistor is much more less in GDI as compared to McCMOS All the simulation results are carried out by using tanner EDA tool on 45nm technology.**

Keywords: - GDI, Analysis of GDI, Digital combinational circuits, McCMOS.

I. INTRODUCTION

With the increase in demand of portable digital application, the demand of high speed, low power dissipation and also the compact designing results in number of research efforts. The art of power analysis and optimization of integrated circuits is now appearing in the mainstream digital design community affecting all aspects of the design process [3]. Full Adder plays a dynamic role in many applications such as image processing, Application Specific ICs (ASICs), video processing etc. By increasing the performance of any full adder will greatly impact on the performance of the entire system i.e. increasing the speed of the whole system. VLSI designer use speed as the performance metric. Hence it is necessary to cognizance of full adder with low power and high performance. Generally, small area and high performance are two contradictory constraints [1]. It was also observed that power efficiency cannot be achieved without affecting the other figures of merits of the design. In CMOS circuits, the power consumed is proportional to changing frequency, load capacitance and the supply voltage [2].

$$\text{Power consumption} = cfV^2$$

Therefore, for increasing the performance of the full adder a design is proposed using two different technique i.e. gate diffusion input and multi-channel length CMOS. Gate diffusion technique is a low power design which allows implementation of various complex logic function by simply using two transistors i.e. maintain low complexity and results in reducing power dissipation, propagation delay and area of digital circuit. Where the multi-channel length CMOS is a technique in increased channel length is used to control the leakage current. The consequence of channel length on threshold voltage (and leakage) is understood as V_{th} decreases quickly as effective channel length (L_{EFF}) is minimized [4]. The organization of the paper is as follows: section II presents basic GDI technique; Section III detailed analysis of GDI; Section IV describes leakage control using McCMOS; Section V, section VI shows simulation and results; and section VII comprises of conclusion.

II. GDI TECHNIQUE

The GDI technique was first offered in 2001 by A. Morgenshtein, A. Fish, and I. A. Wagner [5], which uses a simple structure as shown in figure 1. At first sight, this beginning structure reminds us an ordinary CMOS inverter but there are differences firstly, the GDI structure have three inputs as shown G, P and N where G is common gate input of nMOS and pMOS, P is input to the source/drain of pMOS and N is input to the source/drain of nMOS. It can be arbitrarily biased at contrast with a CMOS inverter.

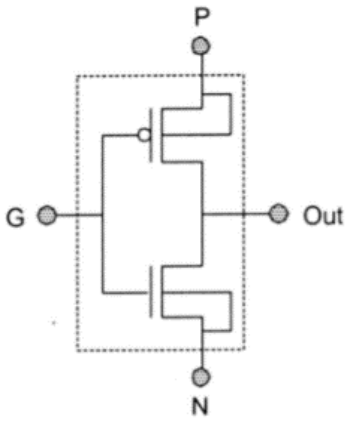


Figure 1: GDI Basic Structure

TABLE I
Logic Functions for different input Configuration of GDI

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	Y1
B	'1'	A	$\overline{A}+B$	Y2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

By simply changing the input configuration number of Boolean functions can be implemented using this simple structure of GDI as shown in the table I. Usually these complex function having 6 – 12 transistors in CMOS, but while using GDI it only require 2 transistors. Implementation on these function will be explained in section V.

Most of the circuit design are based on Y1 and Y2 functions because of the following reasons, both Y1 and Y2 allows realization of any two input logic function i.e. they are complete logic family, Y1 is the only GDI function that can be realized in a standard p-well CMOS process, because the bulk of any nMOS is constantly and equally biased, when N input is at logic high and P input is at logic low then there is a short between N and P results in static power dissipation and $V_{out} \approx 0.5V_{DD}$

Which causes a drawback for implementing OR, AND, and MUX in regular CMOS with configuration. This effect can be minimize if we perform design in floating-bulk SOI technologies [6], where a full GDI library can be employed.

III. ANALYSIS OF GDI

The operational analysis of a basic GDI structure is explained is this section, to understand the effect of low swing in GDI let us consider function Y1 (figure 2) and the same analysis can be extended to use in other GDI function. As shown in the table II that the low swing output will occur when the input values are A=0, B=0. In this case, voltage level of Y1 will be V_{Tp} while the expected voltage level is 0V this is because of the high-to-low switching characteristics of pMOS transistor [7].

TABLE II
Input logic State VS Functionality and output swing of Y1 function

A	B	Function	Y1
0	0	pMOS transGate	V_{tp}
0	1	CMOS Inverter	1
1	0	nMOS Trans Gate	0
1	1	CMOS Inverter	0

Hence this obvious effect will occur during the transition from A=0 B=V_{DD} to A=0 B=0. In some cases, when value of V_{DD}=1 without a swing drop from the last stage, GDI functions as inverter buffer and recovers the swing.

IV. McCMOS TECHNIQUE

Today, high performance CMOS design requires extremely short channel transistor and lowest supply voltage approximately equal to 1V, in order to achieve maximum performance while maintaining power and heat dissipation down to acceptable levels. And all the above is achieve by the use of low threshold transistor which results in increased leakage current. Such increase in the leakage current, leakage power also increases which seems the major problem in sub-micron CMOS design. Hence, an effective leakage control and performance optimization technique McCMOS was introduce. According to McCMOS, leakage current is control by increasing channel length. Doubling up the channel length gives us a leakage saving ratio of order of 250 [8]. The two design principles that describes the channel length Vs leakage relationship are [9] first, in the non-critical path of a circuit the channel length of at least one of the transistor should be increase (preferably one having high probability of turned off) with each possible current path between V_{DD} and gnd. Second, in critical path, similar technique is used but as per necessity increasing transistor width to maintain performance.

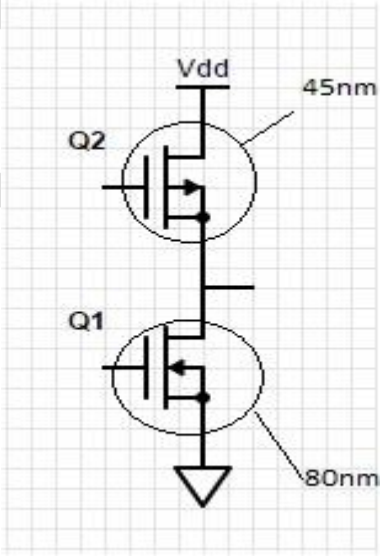


Figure 2: Inverter having 45nm technology using McCMOS

Figure 2 shows the inverter with McCMOS technique for power, speed and performance optimization of the circuit. The model file used here in this paper is 45nm MOS model file. For controlling the leakage power, the non-critical path of the circuit is using non minimum length of nMOS. In critical path, channel length is kept minimum (45nm) while increasing the channel width of pMOS to satisfy the necessary performance.

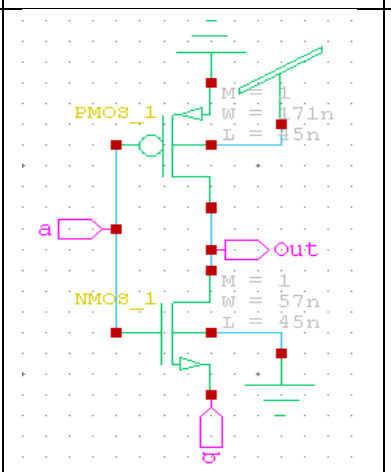
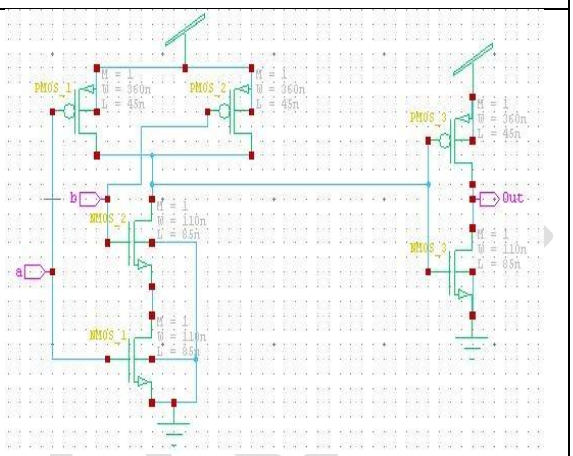
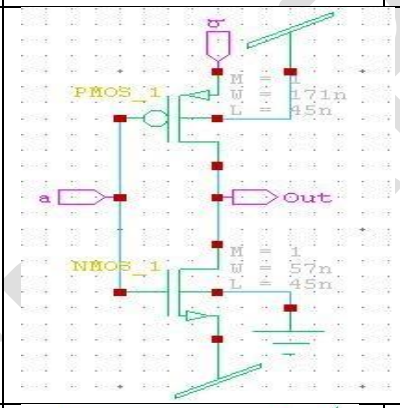
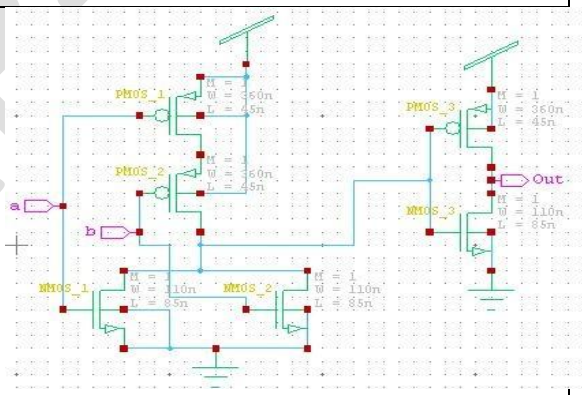
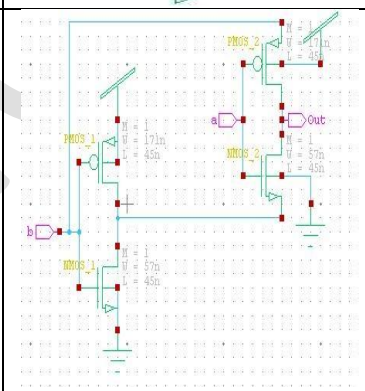
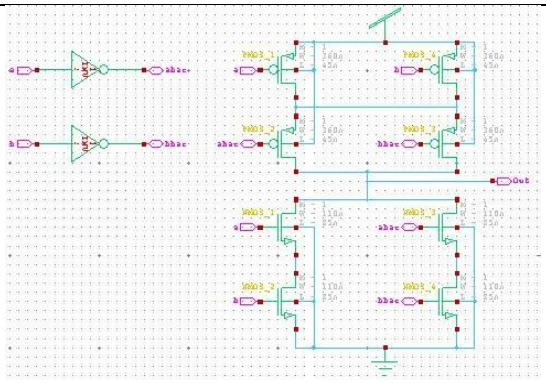
V. SIMULATION

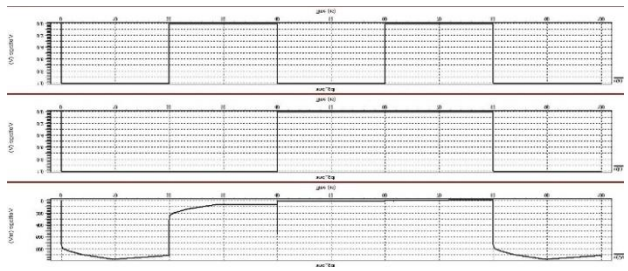
The simulation results show the power and delay of the full adder design. In this all the timing delay and power are extracted and comparison of two technique is shown in the table III using TANNER Tool 14.1 for design implementation and for simulation. Simulation results are performed based on 45nm CMOS technology. The power supply is 1V. The performance assessment is made with

respect to propagation delay, average power, power delay product, the transistor count by GDI and McCMOS. The resulting wave form of is as shown in figure 3 and figure 4.

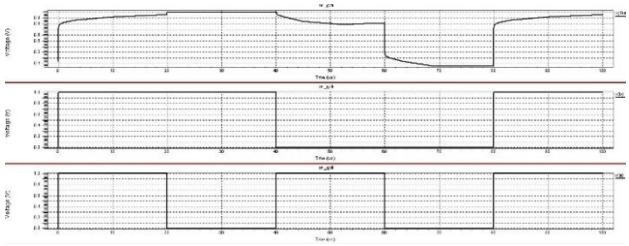
TABLE III

AND, OR and XOR STRUCTURE USING GDI AND McCMOS DESIGN TECHNIQUE

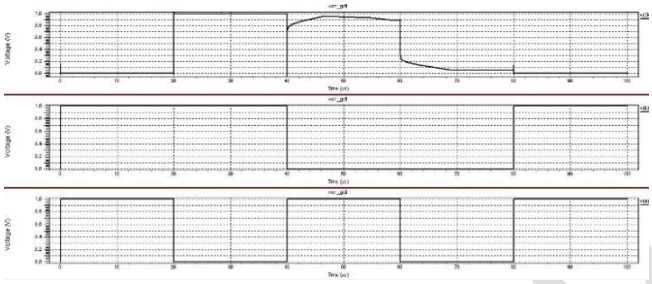
	GDI	McCMOS
AND		
OR		
XOR		



(a)

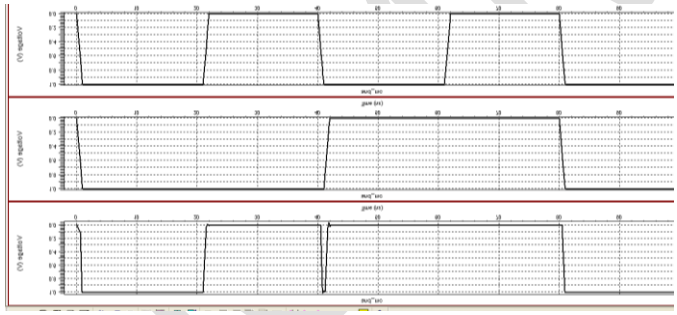


(b)

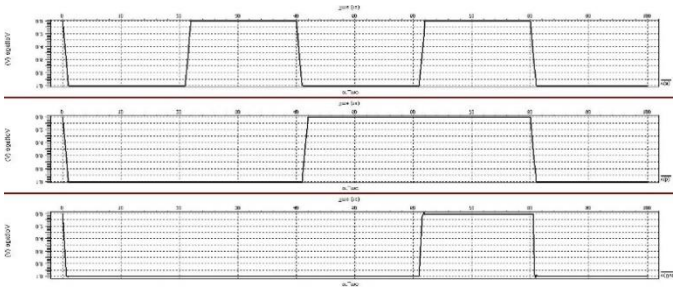


(c)

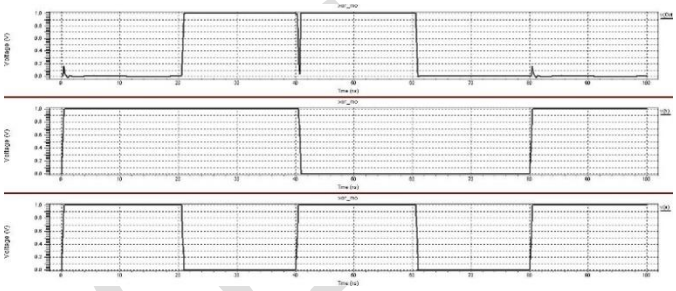
Figure 3: output waveform of GDI (a) AND (b) OR (c) XOR



(a)



(b)



(c)

Figure 4: output waveform of McCMOS (a) AND (b) OR (c) XOR

The circuits have been analyzed in terms of power dissipation, propagation delay and PDP. The term PDP represent product of power delay. Although, both are low power and high speed techniques but it is observed that McCMOS style of designing have 8.09% less power dissipation and approx. 10.5% reduced pdp as compare to GDI in a full adder design. Also, the total number of transistor count is less in GDI as compare to McCMOS although some GDI circuits needs swing restoration to improve its output voltage level and it can be achieve by buffer insertion.

GDI full adder uses only 8 transistor where as McCMOS full adder designed with 42 transistors (using half adder as shown in figure 5), which results in less Table V shows relative performance of GDI and McCMOS based full adder in terms of power dissipation, delay, transistor count, and PDP values.

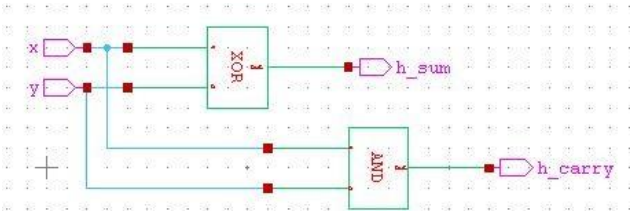
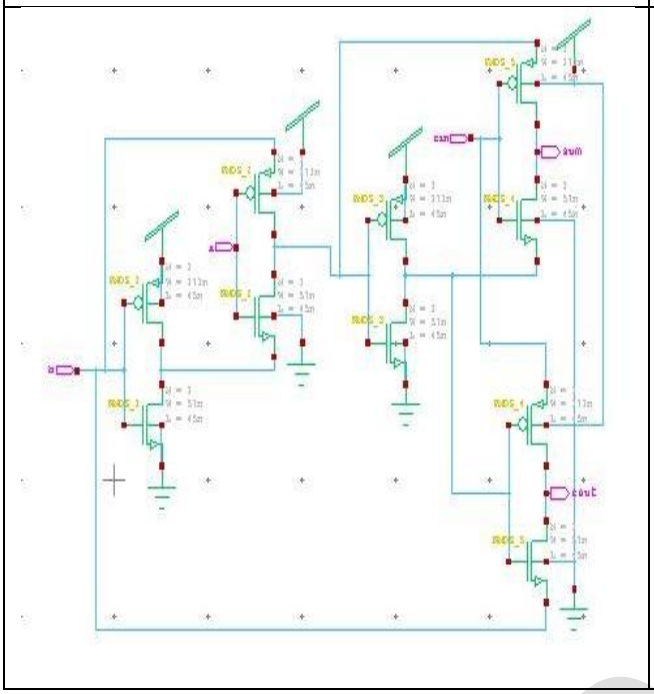
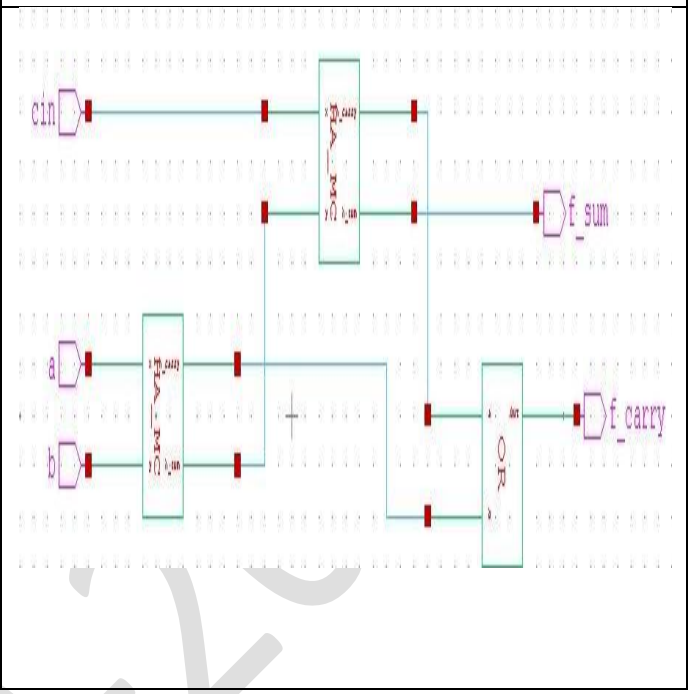


Figure 5: half Adder

TABLE IV

Full Adder design Using GDI and McCMOS

GDI	McCMOS
	

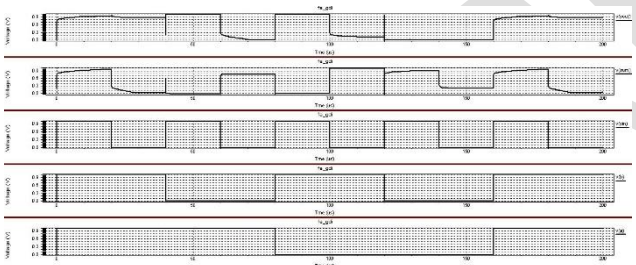
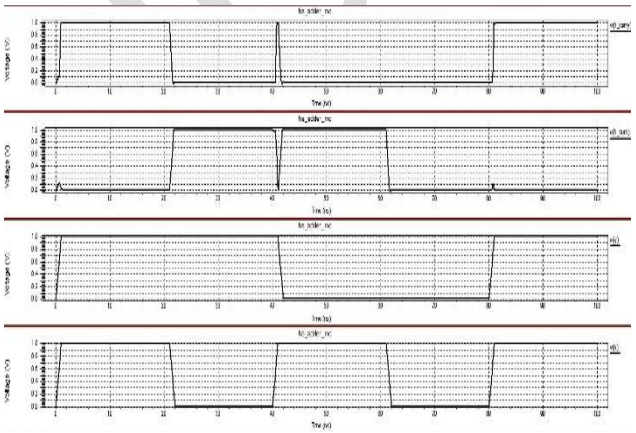
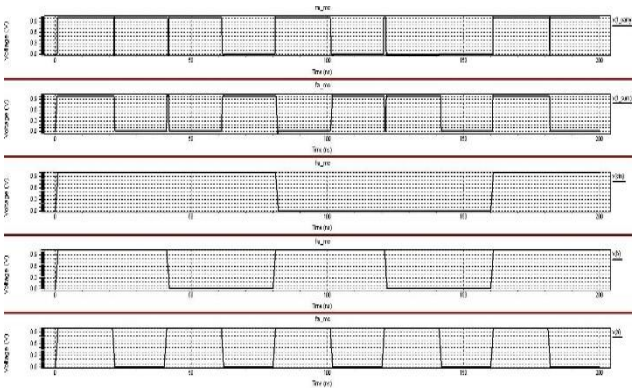


Figure 6: Full adder using GDI



(a)



(b)

Figure 7: Using McCMOS (a) half adder (b) Full adder

VI. RESULT

The comparison performance is analysed, as shown in the table V. On comparing we observed that the average power of the digital circuits is less in McCMOS as compare to the GDI. But the power delay product of gate diffusion technique is small as compare of McCMOS.

Also the number of transistor is less in GDI as compare to McCMOS. Figure 8 and figure 9 show the comparison graphical between the terms delay power, delay and the PDP calculated using GDI and McCMOS.

TABLE V

Comparative Performance Analysis of GDI and McCMOS

	GDI				McCMOS			
	Power (10^{-9}w)	Delay (10^{-9}s)	Pdp (10^{-16}J)	No. of transistor	Power (10^{-9}w)	Delay (10^{-9}s)	Pdp (10^{-16}J)	No. of transistor
AND	3.81	20.5	.781	2	3.23	2.00	6.46	6
OR	14.2	20.4	2.91	2	13.5	2.12	2.86	6
XOR	96.2	.620	.597	2	44.3	1.07	.0476	12
FULL ADDER	1350	20.5	277	8	1270	2.12	249	42

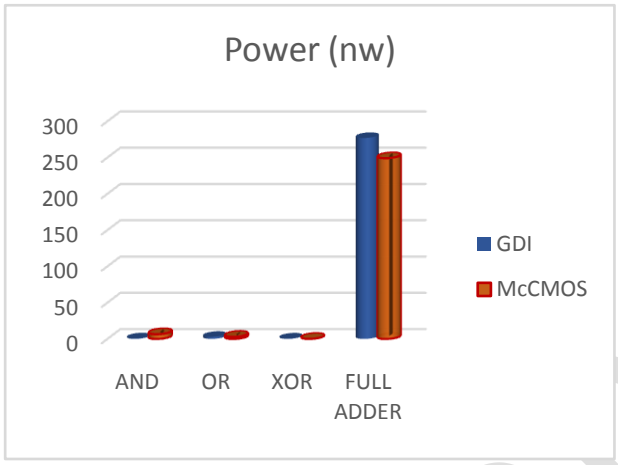


Figure 8: Comparison of Power in different digital circuit

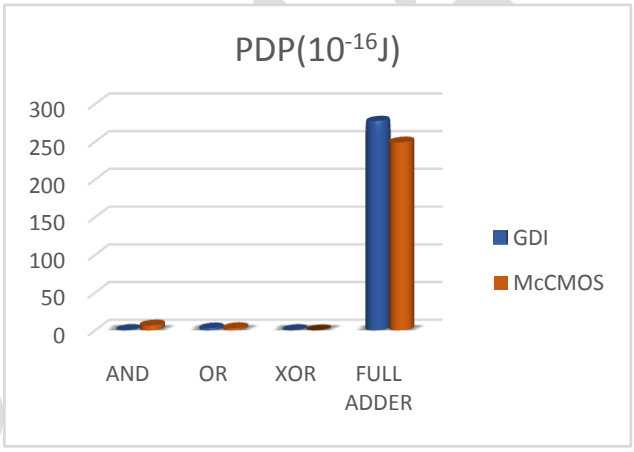


Figure 9: Comparison of PDP in different digital circuit

VII. CONCLUSION

The main aim of designing full adder using these two technique is to reduce power and increase speed. In can be conclude that Even though both are low power and high speed techniques but it is observed that McCMOS style of designing have 8.09% less power dissipation and approx. 10.5% reduced pdp as compare to GDI as McCMOS control the leakage current and hence the performance is improved. But it is also observed that number of transistor is much more less in GDI as compare to McCMOS. These results are obtained with tanner EDA tool Tspice simulation from the extracted net for normal parameters, room temperature and power supply at 1v.

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