

# OFDM Transceiver Implementation using VHDL

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**Abstract—** Orthogonal frequency division multiplexing (OFDM) is a multicarrier modulation technique which is deployed in modern communication systems because of its immunity to channel's harsh affects. Radix-2 ifft butterfly algorithm is used to implement the IFFT block. The system is designed using VHDL and simulated using MODELSIM Altera.

**Keywords-** IFFT, OFDM, VHDL

## I. INTRODUCTION

Orthogonal frequency multiplexing division is a modulation technique in which closely spaced multiple sub carriers are generated using the frequency division of available spectrum. The sub-carriers generated are orthogonal to each other to prevent interference between the closely spaced narrow band sub-carriers. OFDM is mainly implemented to combat harsh and severe channel conditions such as high frequency attenuation and frequency selective fading because such effects are negligible on narrowband signals. A kind of channel equalization is thus obtained because of modulation of several narrow band signals rather than the wideband signal.

A simple OFDM system as shown in Fig 1 consists of a transmitter containing serial to parallel converter, QPSK mapper, IFFT block, DAC and a receiver containing ADC, FFT block, QPSK de-mapper and a parallel to serial converter.

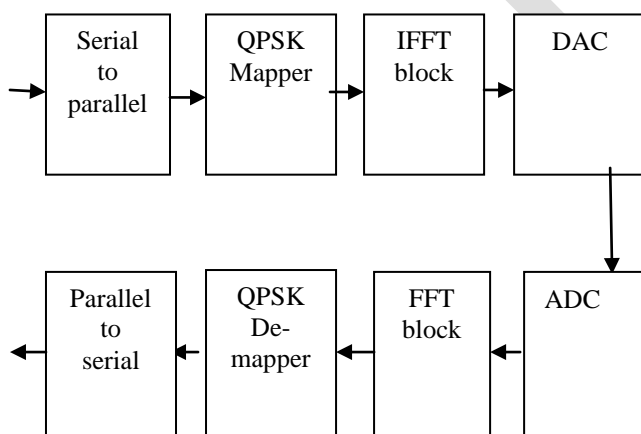


Fig 1 OFDM block diagram

This paper is organized in the following manner. Section II describes the butterfly algorithm; Section III presents the design flow to implement an OFDM transceiver system design. The implementation aspects of the transmitter and receiver are demonstrated in section IV. The equations are discussed in

section V and the result is given in section VI. Finally the conclusion is given in Section VII.

## II. BUTTERFLY ALGORITHM

A simple IFFT algorithm with radix-2 butterfly structure is shown in Fig 2.

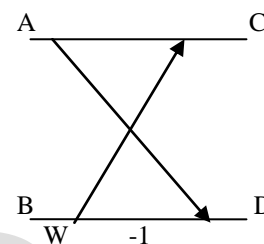


Fig 2 Radix-2 butterfly structure

Here the inputs are A and B and the outputs are C and D. There is a twiddle factor W. The input and output is related as:

$$C = A + WB$$

$$D = A - WB$$

Where,

$$W = e^{-j2\pi/N}$$

Using this algorithm a radix-4 IFFT is implemented in the following manner:

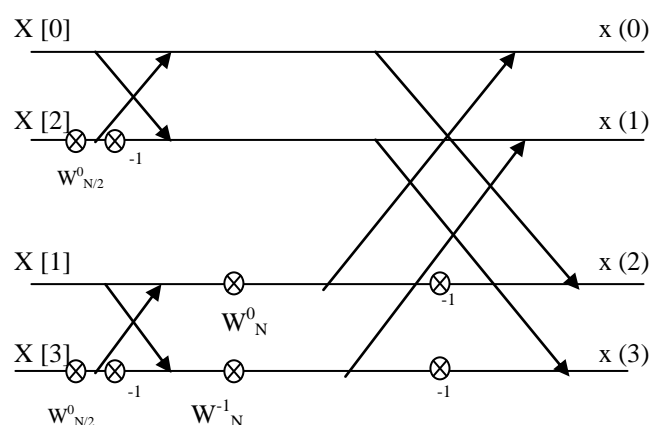


Fig 3 Radix-4 butterfly structure

On the left side we have the frequency domain signals which may be complex or real depending on the input fed to IFFT block and the output on the right side is time domain signal which also can be real or imaginary.

### III. DESIGN FLOW

Initially a serial to parallel converter is implemented using VHDL and simulated separately. After this a transceiver is implemented using VHDL and later unit (i.e. serial to parallel) is merged with this transceiver unit using structural type of modeling. The system is designed using 4-subcarriers.

The system designing starts with the understanding of various units comprising the whole system. The algorithm is implemented using various sequential and concurrent statements. To process the incoming data in parallel, the architecture is broken into various processes.

The project is developed using ALTERA's QUARTUS II project navigator using VHDL coding. Finally the system is simulated using MODELSIM ALTERA.

### IV. TRANSCEIVER DESIGN

At first in the receiver part a stream of 8 bits is taken as input and this stream of bits is converted to parallel data. This process is done independently and the VHD file is linked with the rest of the system using structural modeling. The parallel bit stream is then grouped in a pair to map them in the constellation of QPSK. Separate signals are assigned for processing real and imaginary parts of the mapped signals. A input to output relation is prepared using the butterfly structure algorithm for IFFT calculation.

The output of IFFT block is again resolved into real and imaginary parts and separate signals are assigned to them. The input bit pair is checked and accordingly proper equation is synthesized for the output.

In the receiver section the output of IFFT block is again processed using the radix-4 butterfly algorithm of FFT. Finally the real and imaginary part of output from the FFT block is de-mapped using the same scheme used in QPSK mapping and corresponding bit pair is thus obtained. These bit pairs are separated and converted to parallel data.

### V. EQUATIONS

The equation of four outputs of radix-4 butterfly algorithm for IFFT came out to be as follows:

$$x(0) = X[0] + W_{N/2}^0 * X[2] + W_N^0 * (X[1] + W_{N/2}^0 * X[3])$$

$$x(1) = X[0] + W_{N/2}^0 * X[2] + W_N^{-1} * (X[1] - W_{N/2}^0 * X[3])$$

$$x(2) = X[0] + W_{N/2}^0 * X[2] - W_N^0 * (X[1] - W_{N/2}^0 * X[3])$$

$$x(3) = X[0] + W_{N/2}^0 * X[2] - W_N^{-1} * (X[1] - W_{N/2}^0 * X[3])$$

Where,

$$W_{N/2}^0 = e^{j0} = 1$$

$$W_N^0 = e^{j0} = 1$$

And,

$$W_N^{-1} = e^{j\pi/2} = j$$

The equations of four outputs of radix-4 butterfly algorithm for FFT came out to be as follows:

$$X[0] = x(0) + W_{N/2}^0 * x(2) + W_N^0 * (x(1) + W_{N/2}^0 * x(3))$$

$$X[1] = x(0) + W_{N/2}^0 * x(2) + W_N^1 * (x(1) - W_{N/2}^0 * x(3))$$

$$X[2] = x(0) + W_{N/2}^0 * x(2) - W_N^0 * (x(1) - W_{N/2}^0 * x(3))$$

$$X[3] = x(0) + W_{N/2}^0 * x(2) - W_N^1 * (x(1) - W_{N/2}^0 * x(3))$$

Where,

$$W_{N/2}^0 = e^{j0} = 1$$

$$W_N^0 = e^{j0} = 1$$

And,

$$W_N^1 = e^{j\pi/2} = -j$$

### VI. RESULTS

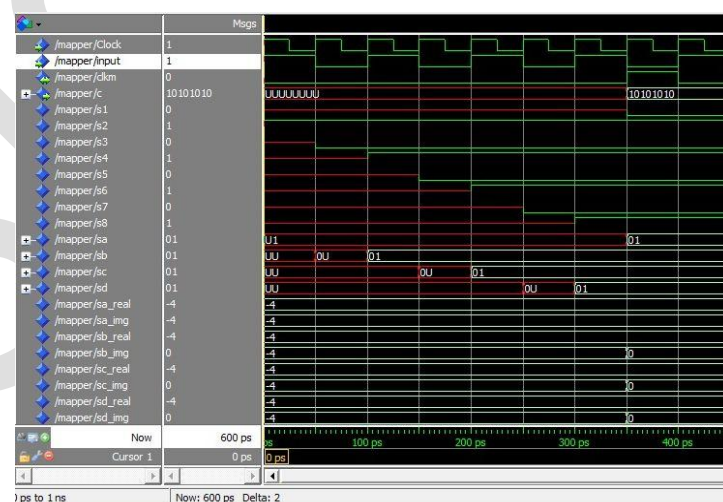


Fig 4 Result of bit stream "10101010"

The results are tested using MODELSIM ALTERA. Ideally the output should be same as the input bits. From Fig 4 it can be seen that the input stream "10101010" is detected correctly and shown as output c. The input bits are read upon rising of the clock and upon detection of 8 bits another clock (i.e. clk) becomes '1'.

From the results it can be seen that proper pairing of bits is done in the signal vectors sa, sb, sc and sd.

### VII. CONCLUSION

The main aim of this paper is to implement OFDM system using VHDL. The system design flow and associated results are discussed in this paper.

From the results it can be concluded that the system is working properly. Also as number of sub carriers increases the number of calculations associated with IFFT and FFT also increases with an increase in spectral efficiency of this system.

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## REFERENCES

- [1]. S. Chavan , P. S. Kurhe , K. V. Karad, "FPGA Based Implementation Of Baseband OFDM Transceiver Using VHDL", Vol. 5 (3), 2014, 4446-4449
- [2]. M.A. Mohamed1, A.S. Samarah1, M.I. Fath Allah2, "Implementation of the OFDM Physical Layer Using FPGA", Vol. 9, Issue 2, No 2, March 2012 ISSN (Online): 1694-0814
- [3]. Manjunath Lakkannavar, Ashwini Desai, "Design and Implementation of OFDM (Orthogonal Frequency Division Multiplexing) using VHDL and FPGA", ISSN: 2249 – 8958, Volume-1, Issue-6, August 2012

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