A Comparative Study of Sub-Threshold Swing for Different TFET Structures Performance of TFET Device

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Abstract: In the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), the sub-threshold swing is limited and it is one the designing parameters of the device. To reduce the scaling problem in the MOSFET, a Tunnel Field Effect Transistor (TFET) is used. The important performance parameters of the device is Sub-threshold Swing (SS), Drain Induced Barrier Lowering (DIBL) etc. For the MOSFET device and further scaled device have to reach 60 mVolt/decade or less than 60 mVolt/decade. In this paper, we study about the Sub-threshold Swing of the Bulk MOSFET and further scaled down devices. The simulation is done for bulk TFET, Source Pocket TFET and Ge Source TFET. The simulation is done in Cogenda T-CAD Version 1.7.4-5. In this paper, the simulation is done for the ultra low power applications i.e. Vdd= 0.01 volt and Vg = -0.1 to 0.5 volt. The gate length of the device is 40 nm and 1nm gate oxide thickness, 100 nm sub-strate thickness. By the simulation, we did competitive study of the Sub-threshold Swing of different devices. We got the good SS for the planner Structure of Ge source TFET. The total fabrication is done for all device on the intrinsic silicon film (n_i= 1E15 cm^{-3}).

Key words: ***MOSFET, TFET, Sub-threshold Swing, DIBL, Source Pocket, T-CAD, Ge source, planner structure.***

I. INTRODUCTION

Tunnel Field Effect Transistor is the best transistor design for low power application[1]. The performance of TFET is improved by band-to-band tunneling and get higher ON current and good sub-threshold swing. Recently experiment shows that Si-TFET[2] and Ge-TFET[3,9] have shown good performance parameters. The Ge-Source design achieves a good ON current due to it's smaller band-to-band tunneling[4]. In [4], the planner Ge-Source TFET is presented. In the MOSFET, the major problem is small ON current, high sub-threshold slope, high DIBL(Drain Induced Barrier Lowering), which is due to scaling down the devices. The better performance is achieved via improving ON current, OFF current, I_{ON}/I_{OFF} ratio and Sub-threshold slope. In the scaled down devices, the sub-threshold slope is 60 mvolt/decade[5]. The performance (switching performance) of the device is improved by minimization of the value of sub-threshold slope (ss).

II. SUB-THRESHOLD SLOPE

The Sub-threshold Swing(ss) of the device is defined as the required the applied gate voltage to increase the one decade output current. The Sub-threshold Slope is defined as[7],

$$SS = \left(\frac{d \log Id}{dVgs}\right)^{-1} \text{ ----------[1]}$$

The Sub-threshold Swing of the MOSFET is limited by diffusion current physics of the device in weak inversion for minimum possible swing in an ideal device is[1],

$$SS_{TFET} = \frac{Vgs^{2}}{5.75\,(Vgs + Const.)} \text{ -----[2]}$$

The value of the sub-threshold swing is limited up to 60 mvolt/decade at room temperature (300 K). From the equation (1&2), indicated that the sub-threshold slope is dependent on the gate voltage and drain current for the small scaled devices.

III. DEVICE STRUCTURE AND SIMULATION PARAMETERS

The simulation is done for planner structure of Ge source TFET, Bulk TFET and Packet source TFET is shown in the Figure(1). The design parameters are listed in Table 1 for the device structure for 40-nm channel length.

IV. COMPARISON OF SUB-THRESHOLD SWING

The sub-threshold swing of the different device such as Bulk TFET, Source Pocket TFET and Raised Source TFET. The sub-threshold swing is measured with the help of the equation(1).

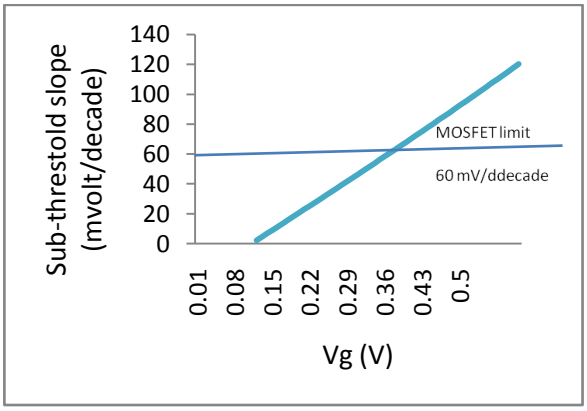
A. Bulk TFET: For the bulk Si-TFET, the simulation is done for Vdd=0.01 volt and gate voltage in the range of -0.1 to 0.5 volt

Table 1. The simulation parameters of planner TFET in S\D region

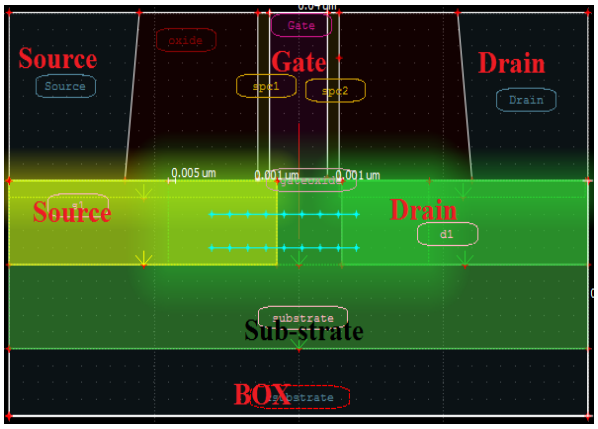
Region	Material	Thickness	Doping (cm^{-3})
Source	P^+ type	25 nm	1E19
Drain	N^+ type	100 nm	1E19
Channel	N type (Si)	100 nm	1E18
Silicon Film	P type (Si)	100nm (including S/D regions)	1E16
Spacer	Nitride	8 nm wide	
Gate oxide	SiO_2	1 nm	
BOX	SiO_2	200 nm	

i.e. for low power applications. The structural parameters and doping in each region is listed in table (1). The thickness of source and drain region is 100 nm and oxide thickness is 1 nm. The Sub-threshold slope is calculated by eq.(1). In figure(1), the structure of Bulk TFET is shown and it's sub-threshold slope is indicating in the figure(1-a) SS Vs. Vgs. As the devices achieves the limit of sub-threshold slope 60 mvolt/ decade quickly than the performance of the device is degraded. In the bulk TFET, the maximum acceptable value for the sub-threshold slope is achieves at 0.37 volt.

B. Pocket TFET: For the improvement of Sub-threshold Slope, the source pocket structure is used[6&8]. The structure and it's SS-Vgs graph is shown in the figure(2 &2a). In this structure, a highly doped packet is fabricated by laser anneling process near to source region[6&8].

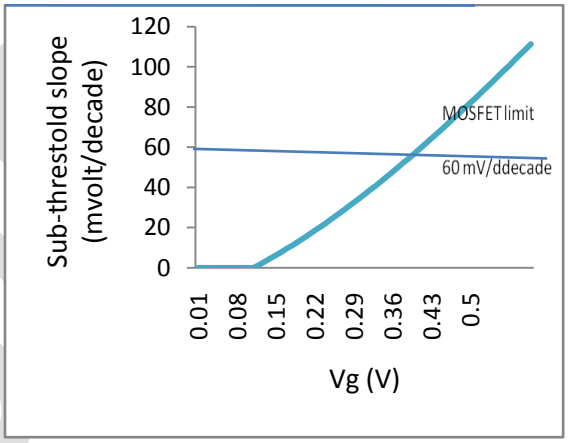


Figure(1) Sub-threshold vs. gate voltage for the Bulk TFET at Lg=40 nm, Vdd=0.01v



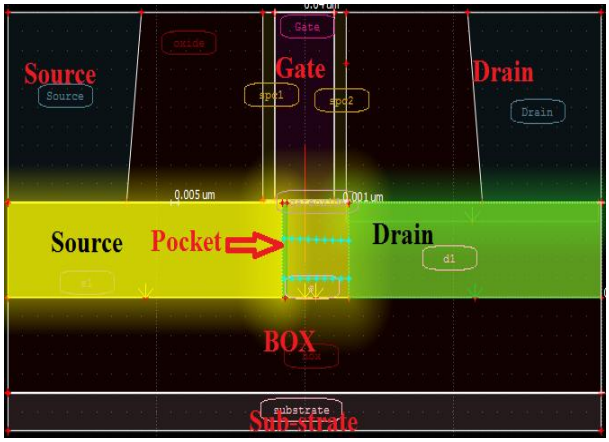
Figure(1a) Cross-section of the Bulk TFET at Lg=40 nm, Vdd=0.01v

In figure(2), the structure of Source TFET is shown and it's sub-threshold slope is indicating in the figure(2-a) SS Vs. Vgs.



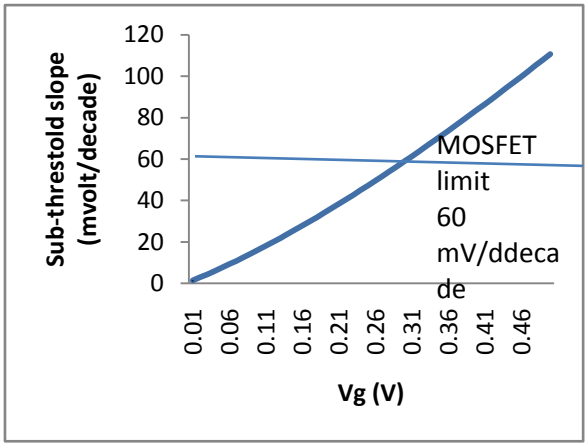
Figure(2) Sub-threshold vs. gate voltage for the Source Pocket TFET at Lg=40 nm, Vdd=0.01v

In the structure of the pocket source TFET, the thickness of the source and drain region is 50nm. The thickness of Silicon substrate is 100nm. In the pocket source TFET, the maximum acceptable value for the sub-threshold slope is achieves at 0.4 volt.



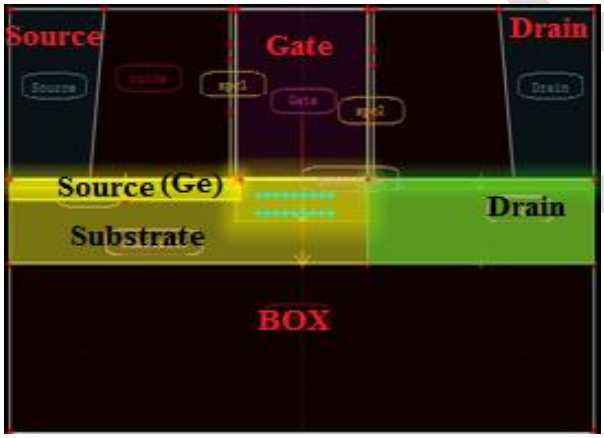
Figure(2a) Cross-section of the source Pocket TFET at Lg=40 nm, Vdd=0.01v

C. Ge Source TFET: In figure(3), the structure of Ge source TFET is shown and it's sub-threshold slope is indicating in the figure(3-a) SS Vs. Vgs. In the Ge Source, the thick Ge is deposited on the Si- source region. The thickness of the Ge layer is 25 nm and Si drain region is 100nm.



Figure(3) Sub-threshold vs. gate voltage for the Ge Source TFET at Lg=40 nm, Vdd=0.01v

The thickness of the sub-strate is 100nm and gate length is 40 nm. In the Ge source TFET, the maximum acceptable value for the sub-threshold slope is achieves at 0.31 volt.



Figure(3a) Cross-section of the Ge source TFET at Lg=40 nm, Vdd=0.01v

V. CONCLUSION

In this paper, the TFET with Ge source is the proper replacement of the ultra low power applications. It shows the steepest sub-threshold slope competitive other TFET's. Steepest Sub threshold slope means the ON-OFF ratio of the device is high and it is beneficial for the ultra low power applications. This analysis is useful to know the switching capacity of the device. Due to good sub-threshold performance, it is used for the switching devices at ultra low power applications.

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