A 45 nm Low Power Two Stage Cmos Operational Amplifier

Ranjan Kumar
Department of ECE
Jaipur National University

Mukesh Maheshwari
Assistant Professor, Dept. of ECE
Jaipur National University

Abstract-**This paper presents the design and implementation of two-stage operational amplifier (Op-Amp). The circuit was designed in PTM 45 nm CMOS process. The design consists of very less number of transistors, hence the design is area optimized. Achieved open loop gain of the amplifier is 76 dB. The unity gain bandwidth (UGB) is 10 MHz and the phase margin is 50 degree with a 10 pF capacitive and 1000K ohm resistive load. High gain enables this circuit to operate efficiently in a closed loop feedback system, whereas high bandwidth makes it suitable for high speed application. The average power consumption of the amplifier is 0.167 µW and slew rate is 8 µ/us.**

Keywords-*CMOS Op Amp, Low Power, Moderate Speed*

I. INTRODUCTION

Operational amplifier is most versatile and basic building block in analog signal processing applications. The operational amplifier (Op-Amp) is a high gain, DC coupled voltage amplifier with a differential input and, single or differential output to be used with negative feedback to exactly outline a closed loop transfer function. The essential requirement for an op amp are sufficiently large open loop gain, large unity gain bandwidth, high input impedance, low output impedance, and high speed. These amplifiers are key elements of most of the analog subsystems, significantly in switched capacitor filters. For previous couple of decades a CMOS implementation of analog circuits established higher than its counterparts because the same technology can be used to implement analog as well as digital building blocks on the same chip. This paper is concentrated on the design of two-stage unbuffered operational amplifier for use within single chip mixed signal system. In section II, the design methodology for two stage CMOS op amp is addressed. In section III, achieved simulation results are presented. Finally, the outcomes of the design are concluded in section IV.

II. DESIGN OF TWO-STAGE CMOS OP-AMP

Currently, the most widely used circuit topology for the implementation of CMOS operational amplifier is the two stage topology. This topology provides good output voltage swing, common mode range, open loop voltage gain, and CMRR. Circuit variations of the basic two-stage amplifier like cascode or folded-cascode topologies can also be used to improve voltage gain further but at the expense of reduced output voltage swing. For a better stability in closed loop applications, frequency compensation is necessary in operational amplifiers. A variety of frequency compensation techniques are proposed to stabilize a closed loop two-stage amplifier [1]-[4]. So as to achieve good stability, other performance parameters are sometime compromised. As a result good compensation technique and design methodology is required to design an op-amp that meets all specifications.

Generic block diagram of straightforward two-stage op-amp is shown in figure 1 below. Initial stage consists of high-gain differential amplifier. Largely cascading is used to enhance the gain during this stage. This stage has the foremost dominant pole of the system. A common source single stage amplifier is typically used as a second stage, which gives high output voltage swing. Third stage is most commonly implemented as the unity-gain source follower circuit [5].

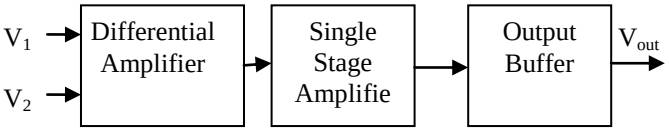

Fig. 1. Block diagram of basic op amp [5]

A. Topology Selection

For high speed and high accuracy circuits, op-amps with high open-loop DC gain, large output voltage swing, and high unity-gain bandwidth are required. Our target is to design and implement an amplifier with 5 MHz unity-gain bandwidth, and a DC gain higher than 73 dB, with a 10 pF load. Topology which will surely enough satisfy this magnitude of DC gain is two-stage topology. Hence two-stage topology is chosen.

B. Design Specifications

The desired specifications of the design are given in the Table I below.

TABLE I. DESIRED SPECIFICATIONS OF THEDESIGNING PARAMETER

Specification	Desired value
DC open-loop gain	≥73dB
Unity gain bandwidth	5MHz
Phase margin	≥60degree
CMRR	≥80dB
Power dissipation	≤2μW
Slew rate	≥10V/μs
Load capacitance	10pF
Load resistance	1KΩ
Load resistance	±1.1V

C. Circuit Analysis and Implementation

The first stage of two-stage op amp is input differential amplifier. Here during this design we tend to used NMOS input pair with current mirror load. NMOS transistors have higher transconductance compared to PMOS transistors, hence NMOS transistors were associate as an input pair. For output stage a common source amplifiers has been used, that is able to provide a higher gain in output stage. The advantage of common source amplifier is high output voltage swing [1]. A complete schematic of op amp is shown in figure 2.

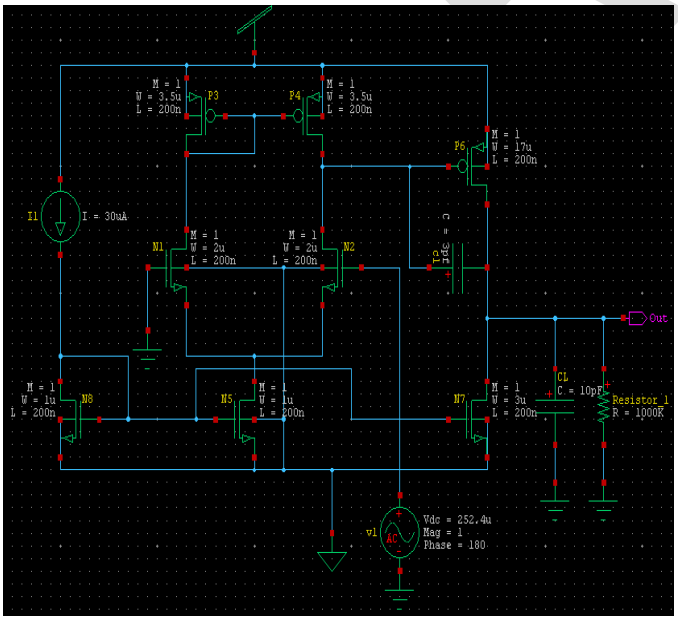

Fig. 2. Schematic of two-stage op amp

All transistors ought to operate in saturation region. Value of compensation capacitor is computed supported load capacitance and unity gain bandwidth requirement for 50° phase margin. Next, the minimum value of tail current I_5 is decided primarily based upon slew rate demand.

In first stage, M1 and M2 are input NMOS transistors, whose transconductance includes a large impact on the open loop gain of the op-amp. Required transconductance (g_{ml} / g_{m2}) of the input transistors is set from the knowledge of compensation capacitance and unity gain bandwidth. Next, the size of M1 and M2 is directly computed from (g_{ml} / g_{m2}). The PMOS transistors M3 and M4 ought to have a high output resistance so that we should get high gain. The scale of M3 and M4 is set by using the requirement for positive input common mode range. Using the negative ICMR equation, overdrive voltage of M5 is calculated, that results in computation of size of M5.

For common source amplifier (second stage) design, the transconductance of M6 is first computed based mostly upon loading pole and unity gain bandwidth measure information. The size of M6 is calculated from size of M3, g_{m3}, and g_{m6}. I_6 may be calculated from the thought of the "proper mirroring" of first-stage current mirror load. I_6 can presumably determine the majority of the power dissipation. The device size of M7 can be determined from size of M5, 1_6 , and I_5. Thus the whole amplifier open loop gain is

$$Av = \frac{2(gm2)(gm6)}{I5(\lambda 2 + \lambda 3)I6(\lambda 6 + \lambda 7)} \quad (1)$$

and total power dissipation is

$$Pdiss = (I5 + I6)(VDD + |Vss|) \quad (2)$$

III. SIMULATION RESULTS

To verify the correctness of the design, many simulations were performed in 45nm CMOS technology using PTM 45 nm library models.

Figure 3 shows the frequency response of op amp. The result shows small-signal voltage gain which is 76 dB and phase margin of 50° which is less than desired value. It can also be seen that the unity gain bandwidth (UGB) of op amp is 10 MHz.

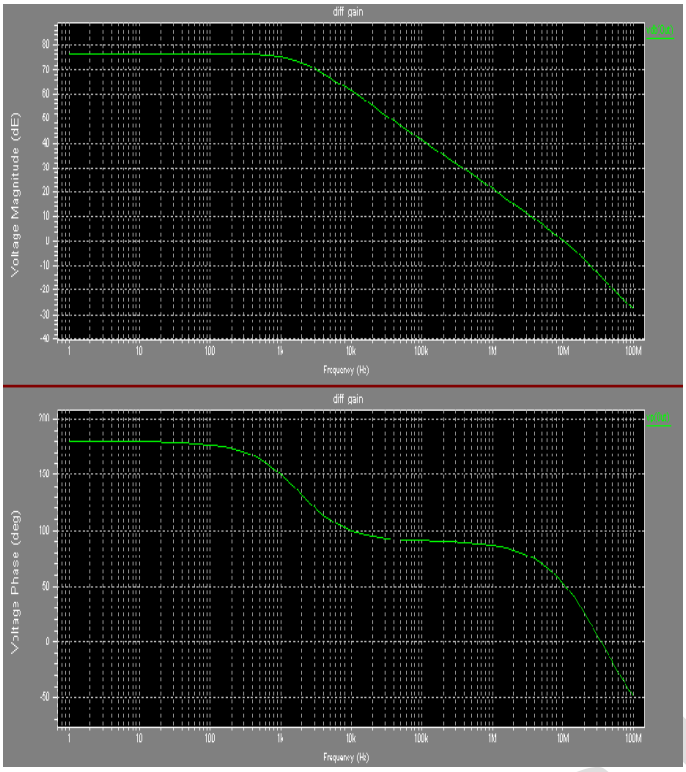

Fig.3. Magnitude and Phase plot of op-amp

A. Common-Mode Configuration Results

The magnitude plots for common mode inputs are shown in figure 4 below. From these plots the measured CMRR is 94 dB. This suggests that op amp has a better rejection to the common-mode noise.

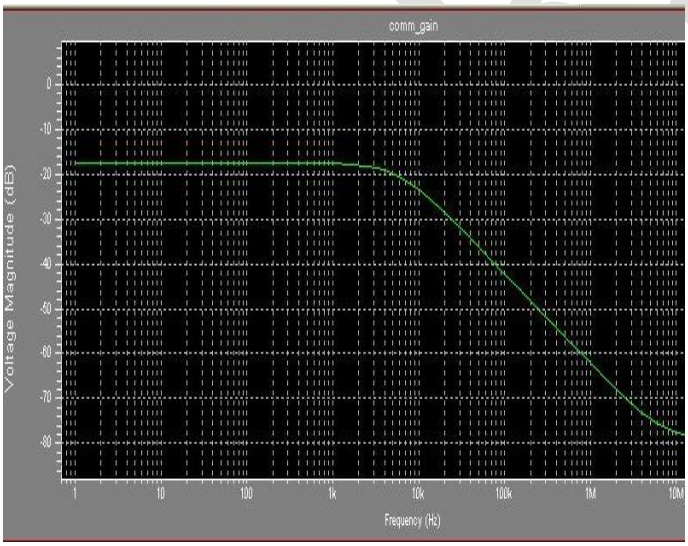

Fig. 4.Common-mode magnitude plot to measure CMRR

The average power dissipation of the op-amp is found after simulation, 0.167µW.

B. Bandwidth

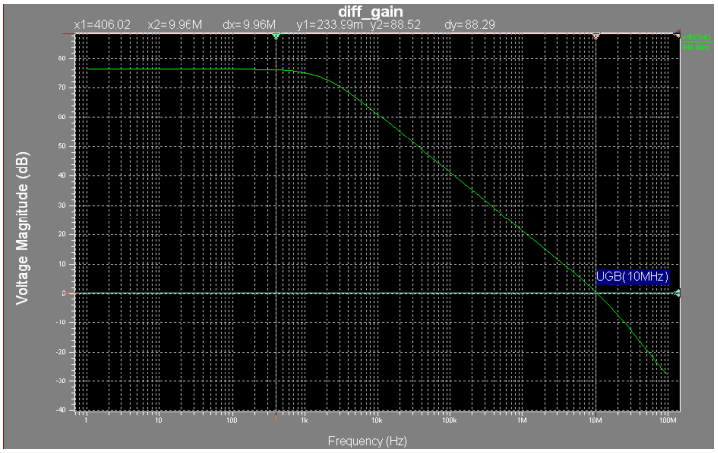

Fig.5. Op-Amp bandwidth

C. Slew Rate

Figure 6 shows the plot to measure positive slew rate. From the plot it can be seen that positive slew rate is $8V/\mu s$, which satisfies the targeted value.

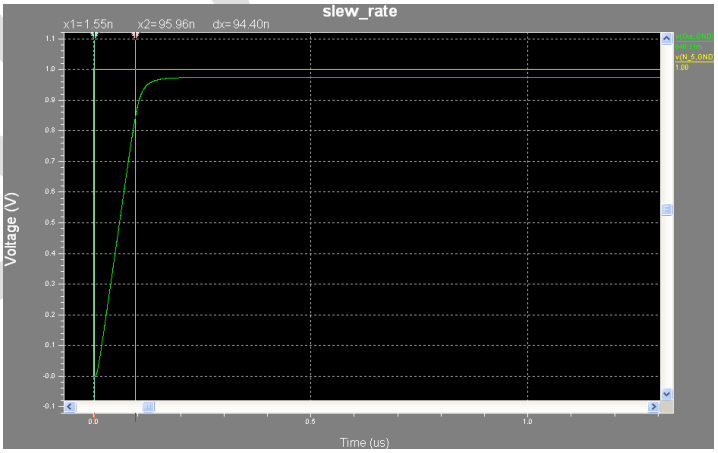

Fig.6. Positive Slew Rate simulation result

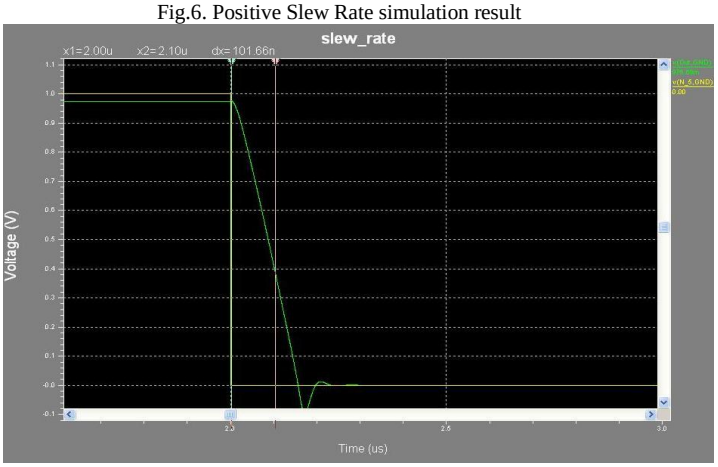

Fig.7. Negative Slew Rate simulation result

Table II below shows the results which have been obtained after simulation. The discrepancies in desired values and obtained values are very less.

TABLE II. RESULTS AFTER SIMULATION

Specification	Desired value	Obtained value
DC open-loop gain	≥73dB	76dB
Unity gain bandwidth	5MHz	10MHz
Phase margin	≥60°	50°
CMRR	≥80dB	94dB
Power dissipation	≤2μW	0.167μW
Slew rate	≥10V/μs	8V/μs
Load capacitance	10pF	10pF
Load resistance	1MΩ	1KΩ
Load resistance	±1.8V	±1.1V

IV. CONCLUSION

Design of op amp is multidimensional optimization problem where optimization of some parameters degrades other parameters. Simulation results make sure that every targeted specifications are achieved except for the phase margin. We can come through higher phase margin by increasing the compensation capacitance however it results in the larger area and more dynamic power dissipation.

Here the improvement in power consumption is achieved by keeping lower tail current which also improves the DC gain of the amplifier. The design achieves slew rate of 8 *V*/μ*S*. Thus it can be considered as a moderate speed op amp.

REFERENCES

[1]. P. Gray and R. Meyer, "Mos operational amplifier design-a tutorial overview," *Solid-State Circuits, IEEE Journal of*, vol. 17, no. 6, pp. 969982, Dec 1982.

[2]. R. G. H. Eschauzier and J. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Springer, 1995.

[3]. G. Palmisano and G. Palumbo, "A compensation strategy for twostage cmos opamps based on current buffer," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 44, no. 3, pp. 257-262, Mar 1997.

[4]. B. Ahuja, "An improved frequency compensation technique for cmos operational amplifiers," *Solid-State Circuits, IEEE Journal of*, vol. 18, no. 6, pp. 629-633, Dec 1983.

[5]. D. R. Holberg and P. E. Allen, *Cmos Analog Circuit Design*. Oxford University Press, 2007.